Web-Based Simulators of
Embedded Software for Programmable Digital Signal Processors

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Outline

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Web-Based System-Level Design Tools

System-Level Design
- Management of complexity and heterogeneity
The Web as an Electronic Design Automation Tool

- Distributed design tools
- Object-oriented design
- Desktop access to the latest tools [WELD]

Synthesis of Efficient Implementations

Implementation Cost Metrics

- Software costs such as data size, program size, throughput, and power consumption
- Hardware costs such as area, weight, throughput, and power consumption

Use of Cost Metrics in Design Space Exploration

- Multiprocessor scheduling [Ptolemy Project Papers] [Architecture Trade Tool]
- Hardware/software codesign [Kalavade and Lee] [POLIS]
- Low-power design [Survey] [Hyper] [Concept] [Pleiades]
- Benchmarking [Berkeley Design Technology]

Embedded Systems

Hidden from the User

Products with Embedded Systems

- Audio CD players and music synthesizers
- Disk drives
- Digital cellular phones
- Sonar and radar
- Video disk players and video telephones

Perform Signal Processing, Communications, and Control

Embedded Software Systems [Graduate Course]
Programmable Digital Signal Processors (DSPs)

Common Properties [Talk on DSP Hardware]

- Fall between microcontrollers and the fastest general-purpose processors in terms of processing power and power consumption
- One cycle execution for most instructions
- Zero-overhead looping
- Hardware multiplier(s)
- Extended precision accumulator
- Separate data and program memory on separate busses
- Special addressing modes
- Various data formats:
  - fixed-point such as the TMS320C50 and Motorola 56000 families (comparison)
  - non-IEEE floating-point such as the TMS320C30 family
  - IEEE floating-point such as the ADSP-21020
- Pipelines with hardware interlocking protection
- Compiler tools are generally not very efficient

Goals for Standalone DSP Simulators

Support System-Level Design Tools

- Leverage existing simulators or disassemblers
- Validate them to be cycle-accurate and bit-true
- Extend them to support different boards and hypothetical configurations
- Return implementation cost estimates
- Make portable across computer platforms
- Report pipeline hazards

Support for Control by a Parent Process

- Separate the user interface from the kernel
- Add hooks to configure the parent process(es) that controls it
- Support pipes by flushing all output

Impact on DSP Simulators

Plans for DSP Simulator Development
### Tools Available by FTP

<table>
<thead>
<tr>
<th>Tools Available by FTP</th>
<th>Simulator Available?</th>
<th>Current Work at UT</th>
<th>Future Work at UT</th>
</tr>
</thead>
<tbody>
<tr>
<td>C30 DSK Tools (1) [Texas Instruments]</td>
<td>No</td>
<td>C30 Simulator (2)</td>
<td>C30 Simulator (3)</td>
</tr>
<tr>
<td>C20 DSK Tools [Texas Instruments]</td>
<td>No</td>
<td>-</td>
<td>C50 Simulator (2)(3)</td>
</tr>
<tr>
<td>56000 Tools [Motorola]</td>
<td>Yes</td>
<td>-</td>
<td>56000 Simulator (2)(3)</td>
</tr>
</tbody>
</table>

1. DSK stands for Digital Signal Processing Starter Kit
2. Will return program, data, and execution time
3. Will return estimates of power consumption

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## The C30 Simulator

### Validation
- Based on the validated disassembler for the C30 DSK board
- Written in C++ that has been run through Purify
- Run simulator in lock step with the C30 DSK board to verify state

### Interaction
- Can be controlled by a parent process
- User can use textual commands

### Portability
- Runs under MS-DOS, Windows, and Unix

### Features:
- Instruction set architecture simulation
- Supports the C30 non-IEEE floating-point format
- Models state of the C30 processor including the pipeline

### Speed
- Simulates about 80,000 C30 instructions/sec on a 167 MHz UltraSparc
- Reasonable for interpreted simulation

### Impact
- First freely distributable C30 simulator
- Changes to the underlying C30 DSK tools have been rolled into C30 DSK tool releases
Impact on Ptolemy

Plans for Incorporating Feedback from Simulators

<table>
<thead>
<tr>
<th>Ptolemy pre-0.7</th>
<th>New in Ptolemy 0.7</th>
<th>Planned for Ptolemy 0.7+</th>
<th>Teamed with</th>
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<tr>
<td>Code Generation (CG) Targets</td>
<td>CG Target Tracks Costs</td>
<td>-</td>
<td>RA, JLP</td>
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<tr>
<td>CG 56000 (CG56) Domain</td>
<td>CG56 Target Tracks Cost</td>
<td>C50 Target Tracks Cost</td>
<td>RA, JLP LG</td>
</tr>
<tr>
<td>CG in C (CGC) Domain</td>
<td>-</td>
<td>CGC/C30 Target Tracks Cost</td>
<td>?</td>
</tr>
</tbody>
</table>

New CG Target Parameters

- Show memory usage?
- Show run time?

Benchmarking of Dual-Tone Modulated-Frequency Decoders [Paper]

Web-Based Design Tools

Web-Based Electronic Design [WELD]

- Finite State Machine Editor
- Schematic Editor for the Synopsys Design Compiler
- Real-Time Package for Java

Tech On-Line DSP Debuggers

- Sluggish telnet access to two C30 boards and two C50 boards
- For demonstration purposes
- No clean way to transfer files

Web-Based Configurable Simulators
Client-Server Architecture

- Java Applets implement the graphical user interface
- Server is written in Java
- Applets communicate with the server over a socket
- Server manages the command-line simulators
- The Applets configure the menus and display based on information returned by the simulator

Web-Enhanced Texas Instruments C30 Simulator (WETICS)

- Tested on Unix platforms and Windows ’95
- Should run on all platforms that support Java
- Release expected in April of 1997
- Preliminary proof-of-concept demonstration installed at UT Austin

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Conclusion

Simulators

- Provide measures of implementation costs
- Cooperate with system-level design tools and graphical user interfaces

Ptolemy Targets Track Implementation Costs

- Ptolemy 0.7 will track software implementation costs for the 56000
- Profiling performance of blocks of C code in systems [Pino]
- Hooks exists for tracking hardware implementation costs

Web-Enhanced, Configurable Users Interfaces

- Simulators
- Debuggers

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