

Hardware Synthesis from SDF

- Start with SDF universe - abstract algorithm design
- Retarget to VHDL if corresponding stars available
- Target generates hardware blocks for individual functions
- Registers for state and for data transfer between blocks
- Initializers and selectors for registers
- Register updates between SDF schedule iterations
- Allows for resynthesis, rescheduling of hardware design

- **Additional Goals**
 - Feedback (back-annotate) info from synthesis to VHDL target
 - Regroup functional blocks to improve synthesis result
 - Generate control, clocks, resets automatically

New domain block style

- Stars written in terms of interface and function
- Macros similar to CGC, but elaborated differently
- Different code generated from same star by different VHDL targets

```
defstar {
  name { Ramp }
  domain { VHDL }
  output { name { output } }
  defstate { name { step } }
  defstate { name { value } }
  codeblock (std) {
    $ref(output) $assign(output) $ref(value);
    $ref(value) $assign(value) $ref(value) + $val(step);
  }
  go {
    addCode(std);
  }
}
```

Future Release Plans

- **No further additions to VHDLF, VHDLB domains**

New VHDL Domain


- **Fully inhomogeneous SDF semantics (multirate)**
- **Generate code in different styles depending on choice of target**
 - Target to generate code for efficient simulation
 - Target to generate code for synthesis
 - Target to use with Synopsys synthesis tools
 - Target to use with Synopsys simulator
- **Co-simulation between Ptolemy and Synopsys**
- **FPGA synthesis and download to target architecture on Sparcstation bus board for rapid prototyping**

Some VHDL Demos

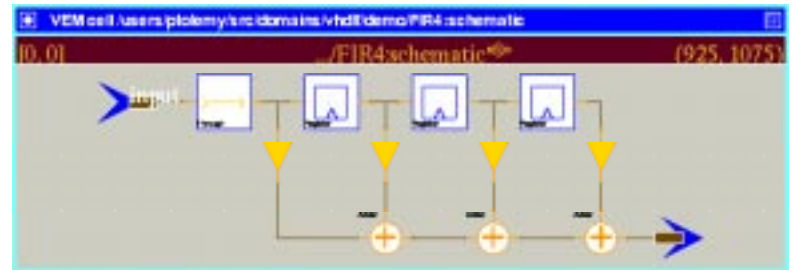
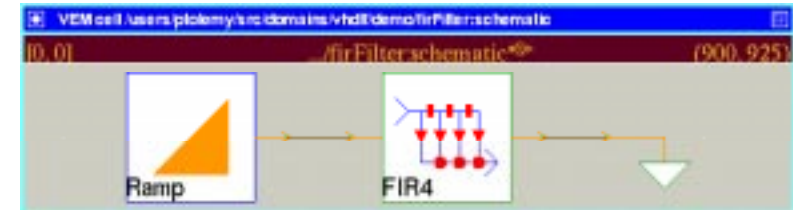
VEM cell / users / ptolemy / vhdldemo / init.pa schematic (1275, 825)

VHDLF Demos

The VHDLF domain is an experimental, and still underdeveloped domain for VHDL code generation for functional blocks with SDF-like semantics.



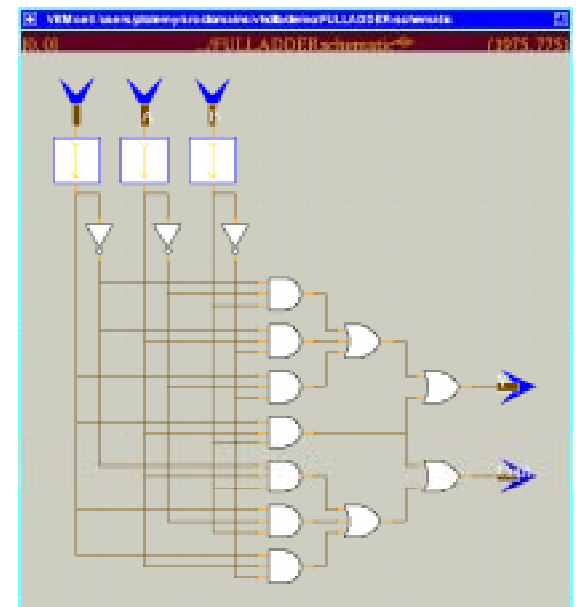

test



VEM cell / users / ptolemy / vhdldemo / init.pa schematic (1550, 950)

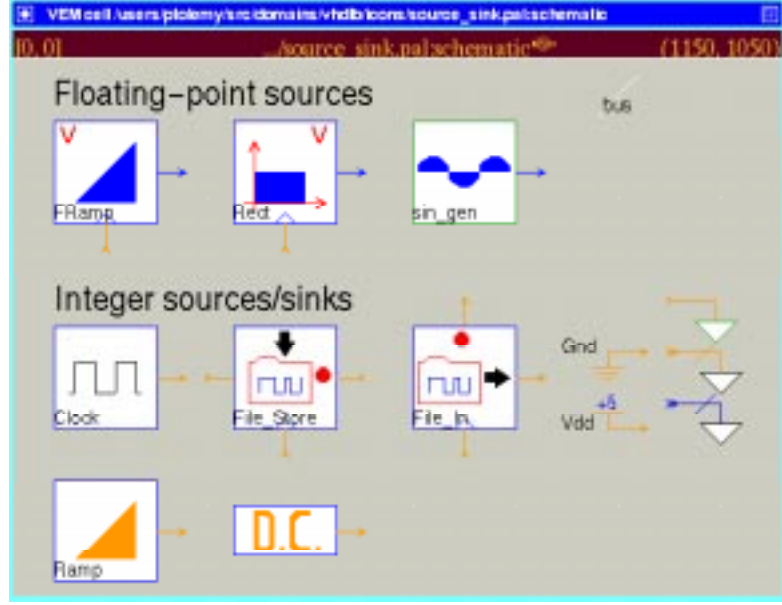
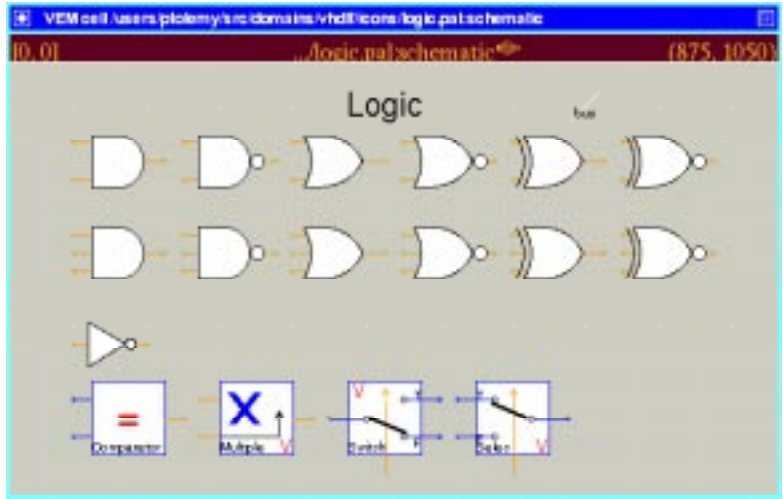
VHDLB Demos

The VHDLB domain is an experimental, and still underdeveloped domain for VHDL code generation for behavioral blocks with DE-like semantics.



Some VHDL Stars

The screenshot shows the 'VHDL Stars' menu in the SPTOLEMY software. The menu is organized into two sections: 'VHDLF Stars' and 'VHDLB Stars'. The 'VHDLF Stars' section includes: Signal Sources and Sinks, Arithmetic, Nonlinear Functions, Logic, Control, Conversion, Signal Processing, Discrete Components, and Demos. The 'VHDLB Stars' section includes: Signal Sources and Sinks, Arithmetic, Nonlinear Functions, Logic, Control, Conversion, Signal Processing, Discrete Components, and Demos. The 'Logic' option is highlighted, and a sub-menu is visible showing various logic components like AND, OR, NOT, and XOR gates, as well as comparators and multipliers.



Steps in VHDL Code Generation

- **VHDLTarget iterates through all blocks**
- **For each block, iterates through all ports**
- **Constructs top-level entity**
- **Instantiates an entity for each star in the graph**
- **Instantiates a signal for each arc**
- **Specifies port connections accordingly**
- **Generates code hierarchically for Ptolemy galaxies**
- **Configuration references to the VHDL code in the library directories**

Writing VHDL Blocks - VHDL Code File

- Corresponding VHDL code file `Vhdlfxxx.vhdl`
- In `$PTOLEMY/src/domains/vhdlf/lib/` directory
- Entity, architecture, and empty configuration

```
entity VHDLFNot is
    port (input: in integer; output: out integer);
end VHDLFNot;
```

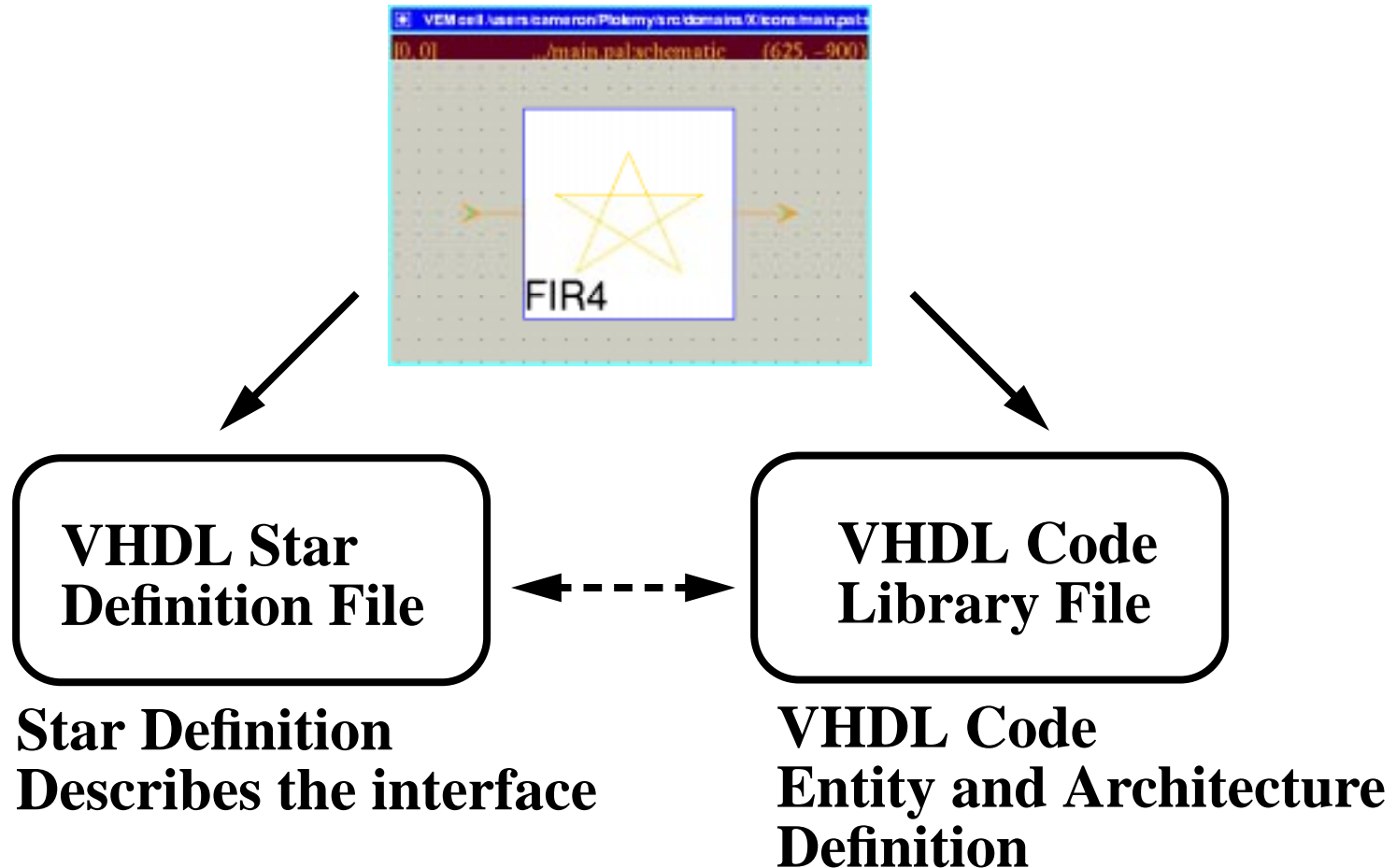
```
architecture VHDLFNot_behavior of VHDLFNot is
begin
    process
    begin
        wait on input'transaction;
        if input /= 0 then
            output <= 0;
        else
            output <= 1;
        end if;
    end process;
end VHDLFNot_behavior;
```

Writing VHDL Blocks - Star Definition

- Star definition file VHDLFxxx.pl
- In \$PTOLEMY/src/domains/vhdlf/stars/ directory
- Describes only the interface: ports, states, datatypes
- Empty go() method

```
defstar {  
    name { Not }  
    domain { VHDLF }  
    input {  
        name { input }  
        type { int }  
    }  
    output {  
        name { output }  
        type { int }  
    }  
    go {  
    }  
}
```

VHDL Block Definition Organization



- Block writer ensures correspondence between the two
- Import existing VHDL code module by writing a star definition for it

Two VHDL Domains in Ptolemy

VHDL-Functional (VHDLF)

- No timing dependency
- Actors compute fixed functions on data streams
- Computations occur at discrete intervals
- Computations occur with zero latency
- Synchronous Dataflow (SDF)-like semantics

VHDL-Behavioral (VHDLB)











- Timing dependency
- Actors may have time-dependent behavior
- Computations may occur at any time
- Computations may have non-zero latency
- Discrete Event (DE)-like semantics

Some CGC Demos

VEM cell / users / ptolemy / src / domains / tgc / demo / init / pal / schematic

(0, 0) /init.pal.schematic (1975, -1375)








CGC Demos
C-code generation demos
for single processor
and multiple processors

-  **Basic** 
-  **Multirate**
-  **Signal Processing**
-  **Multi-Processor Demos**
-  **Fixed-Point Demos**
-  **Sound**
-  **Tcl/Tk**
-  **BDF**
-  **Higher Order Functions**

VEM cell / users / ptolemy / src / domains / tgc / demo / basic / pal / schematic

(0, 0) /basic.pal.schematic (1025, -900)

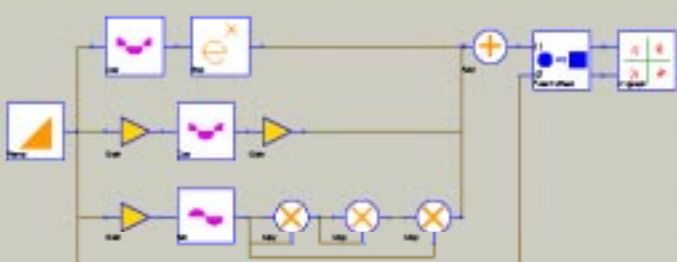
Basic demos illustrating
simple uses of Ptolemy and
the use of certain stars

-  butterfly
-  nonlinear
-  shape
-  integrator
-  turtle
-  characteristics
-  swain-fordson

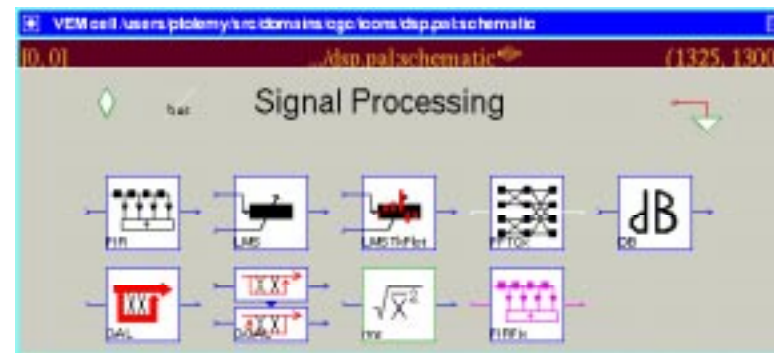
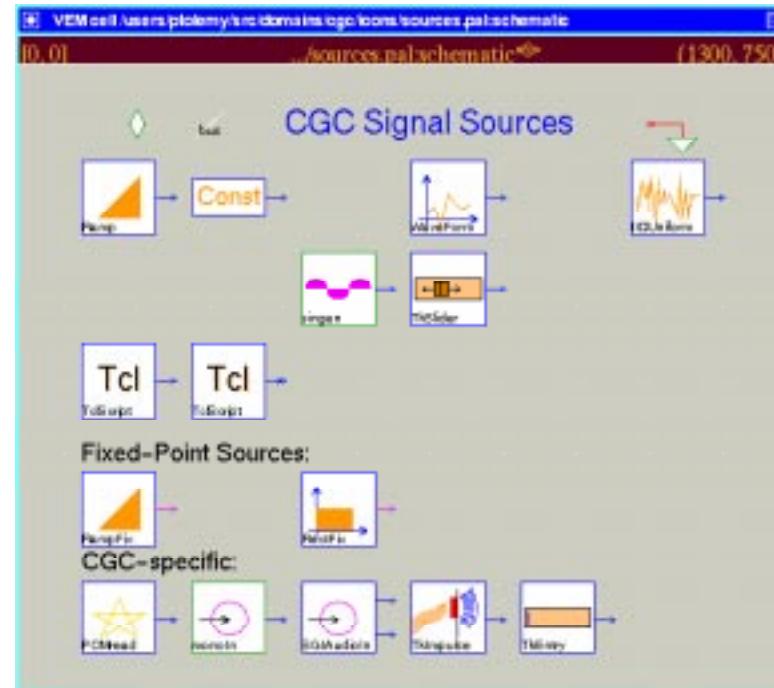
VEM cell / users / ptolemy / src / domains / tgc / demo / butterfly / schematic

(0, 0) /butterfly.schematic (1375, 800)

The Butterfly Curve
(T. Fay, American Mathematical
Monthly, 96(5), 1989)



Some CGC Stars



Tcl/Tk in CGC

- **Tcl/Tk stars in CGC, comparable to Tcl/Tk stars in SDF**
- `TclTk_Target`

Additional Methods for TclTk stars in CGC

- `void errorReport()`
- `void makeEntry()`
- `void makeButton()`
- `void makeScale()`
- `void displaySliderValue()`

BDF in CGC

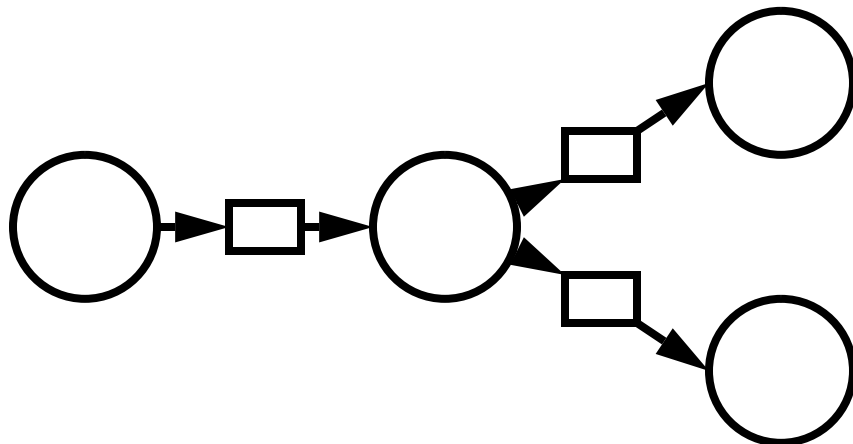
- Use bdf-CGC target
- Two principal stars: switch and select
- `setRelation()` method
 - `DF_NONE`
 - `DF_TRUE`
 - `DF_FALSE`
 - `DF_SAME`
 - `DF_COMPLEMENT`

```
trueOutput.setRelation(DF_TRUE, &control);  
falseOutput.setRelation(DF_FALSE, &control);
```

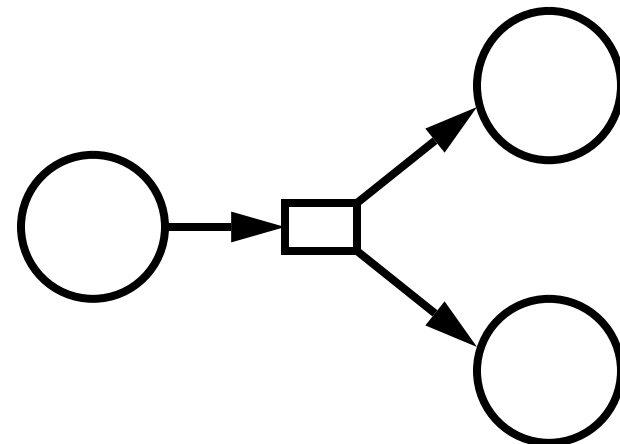
Buffer Embedding

- Data communication across arcs implemented using buffers
- Avoid allocating buffers for certain stars: spread, collect, fork, upsample, downsample (use embedding of static buffers if possible)
- Declare buffer embedding in the setup method

```
setup {  
    input.embed(trueOutput, 0);  
    input.embed(falseOutput, 0);  
}
```



no embedding



embedding

CGC addCode Methods and Streams

Additional methods to add to specific code streams

- `addInclude()`
- `addDeclaration()`
- `addGlobal()`

Additional code streams

- `CodeStream include`
- `CodeStream mainDecls`
- `CodeStream globalDecls`
- `CodeStream mainInit`
- `CodeStream mainClose`

A Small Generated Code File, ctd

```
...
for (i_3=0; i_3 < 10; i_3++) {
    { /* star SmallTest.Ramp1 (class CGCRamp) */
    output_0 = value_4;
    value_4 += 1.0;
    }
    { /* star SmallTest.XMgraph1 (class CGCXMgraph) */
    if (++count_5 >= 0) {
        fprintf(fp_1[0], "%g %g\n", index_6, output_0);
    }
    index_6 += 1.0;
    }
} /* end repeat, depth 0*/
{ int i;
  for (i = 0; i < 1; i++) fclose(fp_1[i]);
  system("( pxgraph -t 'X graph' -bb -tk =800x400
default-CGC_temp_20 ; /bin/rm -f default-CGC_temp_20) &");
}
}
```

A Small Generated Code File

```
#include <stdio.h>

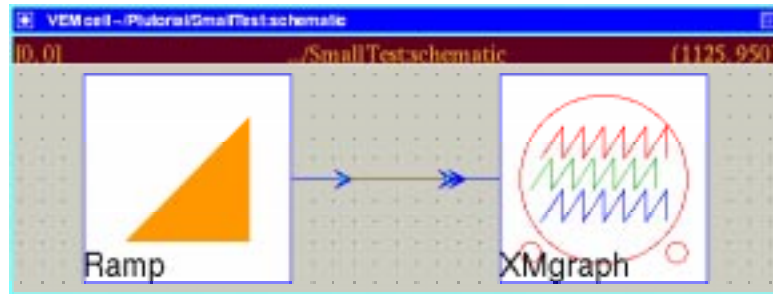
/* main function */
main() {
    FILE* fp_1[1];
    int i_3;
    double value_4;
    double output_0;
    int count_5;
    double index_6;
    count_5=0;
    index_6=0.0;
    value_4=0.0;
    output_0 = 0.0;
    if(!(fp_1[0] = fopen("default-CGC_temp_20","w")))
    {
        fprintf(stderr,"ERROR: cannot open file.\n");
    }
    for (i_3=0; i_3 < 10; i_3++) {
        /* star SmallTest.Ramp1 (class CGCRamp) */
        output_0 = value_4;
    }
}
```

Declarations

Initialization

Init Code

A Small Test System



```

#! /usr/bin/perl -w
# SmallTest: a test system
#
# Usage: perl SmallTest.pl [options]
#
# Options:
#   -h, --help           show this help message
#   -d, --debug          enable debugging
#   -s, --stop=TIME     stop at TIME (default: 10)
#   -o, --output=FILE   output to FILE (default: stdout)
#
# Example: perl SmallTest.pl -d -s 5 -o output.txt
#
# Copyright (c) 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021, 2022, 2023, 2024, 2025, 2026, 2027, 2028, 2029, 2030, 2031, 2032, 2033, 2034, 2035, 2036, 2037, 2038, 2039, 2040, 2041, 2042, 2043, 2044, 2045, 2046, 2047, 2048, 2049, 2050, 2051, 2052, 2053, 2054, 2055, 2056, 2057, 2058, 2059, 2060, 2061, 2062, 2063, 2064, 2065, 2066, 2067, 2068, 2069, 2070, 2071, 2072, 2073, 2074, 2075, 2076, 2077, 2078, 2079, 2080, 2081, 2082, 2083, 2084, 2085, 2086, 2087, 2088, 2089, 2090, 2091, 2092, 2093, 2094, 2095, 2096, 2097, 2098, 2099, 2100, 2101, 2102, 2103, 2104, 2105, 2106, 2107, 2108, 2109, 2110, 2111, 2112, 2113, 2114, 2115, 2116, 2117, 2118, 2119, 2120, 2121, 2122, 2123, 2124, 2125, 2126, 2127, 2128, 2129, 2130, 2131, 2132, 2133, 2134, 2135, 2136, 2137, 2138, 2139, 2140, 2141, 2142, 2143, 2144, 2145, 2146, 2147, 2148, 2149, 2150, 2151, 2152, 2153, 2154, 2155, 2156, 2157, 2158, 2159, 2160, 2161, 2162, 2163, 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```

Generating Code for a Single Firing

Adding one firing's code to the code stream

```
go {
    addCode(std);
}
...
codeblock (std) {
    $ref(output) = $ref(value);
    $ref(value) += $val(step);
}
```

An alternative way to do the same thing

```
go {
    StringList out;
    out << "\t$ref(output) = $ref(value);\n";
    out << "\t$ref(value) += $val(step);\n";
    addCode((const char*)out);
    out.initialize();
}
}
```

Determining Resource Requirements

```
...
defstate {
  name { step }
  type { float }
  default { 1.0 }
  desc { Increment from one sample to the next. }
}
defstate {
  name { value }
  type { float }
  default { 0.0 }
  desc { Initial (or latest) value output by Ramp. }
  attributes { A_SETTABLE|A_NONCONSTANT }
}
...
```

- States will correspond to resources in generated code
- Attributes guide the target in deciding how to allocate resources

Example Star: CGCRamp.pl

```
defstar {
  name { Ramp }
  domain { CGC }
  desc {
    Generates a ramp signal, starting at "value" (default 0)
    with step size "step" (default 1).
  }
  author { E. A. Lee }
  output {
    name { output }
    type { float }
  }
  defstate {
    name { step }
    type { float }
    default { 1.0 }
    desc { Increment from one sample to the next. }
  }
  defstate {
    name { value }
    type { float }
  }
}
```


Outline

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 - Future Release Plans
 - New Domain Block Style
 - Hardware Synthesis from SDF

Writing Blocks for CGC and VHDL



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