White Eagle
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Digital Hearing Aid Design Using Ptolemy

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Purpose of Presentation

- Commercial product development using Ptolemy
- Heart of design is a hard coded DSP algorithm
- Describe how Ptolemy was used to develop a CIC Hearing Aid
- Describe the tool-flow for the development of a hard coded DSP algorithms with Ptolemy
- Describe benefits of the design approach
- Review of bottlenecks in design approach

CIC Digital Hearing Aid Design Constraints

- Physically constrained in size to fit inside the average adults ear-canal next to the ear-drum
  - CIC (Completely-In-the-Canal) Hearing Aid
- Thus gate count must be small even in 0.35µ CMOS technology
- Power must be small to keep battery life reasonable
- Sub 1V standard power source (unusual for standard 0.35µ CMOS technology)
- Design was highly parameterizable (not programmable)
- Development time (as in all projects) was very constrained
- Conclusion: These constraints dictate the need for hard coding the DSP algorithm

Design Flow For Hard-Coded DSP Algorithm Development - 1

- New DSP algorithms are first described as a floating point arithmetic algorithm
  - developed additional floating point SDF stars
- Created test bench and large set of tests to test floating point algorithm (this same test bench and set of tests will be used in all design environments)
- Changed algorithm to fixed point
  - re-built Ptolemy fixed point class
  - re-built Ptolemy galaxy's with fixed point stars
  - used Ptolemy to analyze best precision for each variable in the galaxy
  - re-ran floating point test's to qualify precision's and the fixed point galaxy

Design Flow For Hard-Coded DSP Algorithm Development - 2

- Developed chip architecture
  - SDF graphs show parallel and serial computation paths
  - SDF graphs help greatly in determining best chip architecture for the CIC ASIC
- Implemented chip architecture in Verilog RTL
- Built Verilog test benches that integrated in with the test benches of Ptolemy simulations
  - enabled ability for bit-exact comparison of algorithm
- Parts of the algorithm were accelerated on the WhiteEagle™ hardware accelerator
  - has Tcl/Tk interface that allows data flow testing using the results from Ptolemy runs
  - allowed bit-exact comparison of algorithm on larger sets of data

Design Flow For Hard-Coded DSP Algorithm Development - 3

- Ambit synthesis of Verilog RTL to gates
- Used Verilog test benches and tests to run data over gates
  - this is where bit-exactness really helps
  - ran corner case tests and some normal data tests
  - not feasible to run all test that were done in Verilog RTL
- Normal ASIC flow with ASIC vendor for rest of chip

Benefits of Approach

- Believe using the traditional ‘C’ modeling approach would not have led to a design within the size and power constraints in the time we had to develop the ASIC
  - algorithm structure is best represented as a graph
  - additional modeling tools within Ptolemy environment help with analysis
  - almost all stars used in the CIC ASIC are in Ptolemy
- Hardware accelerator fits easily into a SDF design
  - this was even 1000 times faster than the Ptolemy simulations

Bit-exactness is critical

- Ptolemy fixed point Verilog simulation times are much faster than Verilog RTL and gate level simulation times
- only a subset of all of the Ptolemy tests can be used in the Verilog RTL or gate level simulations
- since the chip simulations are on a smaller subset of tests, bit-exactness builds confidence that the algorithm in silicon is the same as the algorithm we modeled

Bottlenecks in Process

- Process of moving from floating point to fixed point is a manual process
  - we still rely on engineering experience and knowledge of the algorithm
- Fixed point class is very slow in execution
  - this is a major headache for us
  - we are working on a faster CGC like domain
- Translation from fixed point Ptolemy SDF to chip architecture is a manual process
- Verilog simulation of SDF is very slow
  - we used our hardware accelerator, but this isn't always appropriate during development

Summary

- Ptolemy can be used successfully on DSP development projects
- Ptolemy algorithm model greatly helps in the chip architecture definition process
- Ptolemy SDF fixed point simulation speeds chip development by minimizing long running Verilog simulations