References

[Bha93a] S. S. Bhattacharyya and E. A. Lee, "Looped Schedules for Dataflow Descriptions of Multirate Signal Processing Algorithms," *Formal Methods in System Design*, No. 5, No. 3, December 1994 (Updated from Technical Report UCB/ERL M93/37, EECS Dept., UC Berkeley, May 21, 1993).

[Bha93b] S. S. Bhattacharyya, J. T. Buck, S. Ha, and E. A. Lee, "A Scheduling Framework for Minimizing Memory Requirements of Multirate DSP Systems Represented as Dataflow Graphs," *VLSI Signal Processing VI*, ed. by L. Eggermont, P. Dewilde, E. Deprettre, and J. van Meerbergen, pp. 188-196, IEEE Special Publications, New York, NY, 1993.

[Bha93c] S. S. Bhattacharyya, J. Buck, S. Ha, and E. A. Lee, "Generating Compact Code from Dataflow Specifications of Multirate Signal Processing Algorithms," *IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications*, vol. 42, no. 3, pp. 138-150, March 1995 (Updated from Technical Report M93/36, EECS Dept., UC Berkeley, May 21, 1993).

[Bha94a] S. S. Bhattacharyya and E. A. Lee, "Scheduling Synchronous Dataflow Graphs for Efficient Looping," *J. of VLSI Signal Processing*, vol. 6, December 1993.

[Bha94b] S. S. Bhattacharyya and E. A. Lee, "Memory Management for Dataflow Programming of Multirate Signal Processing Algorithms," *IEEE Trans. on Signal Processing*, vol. 42, no. 5, May 1994 (Updated from Technical Report UCB/ERL M92/128, EECS Dept., UC Berkeley, November 18, 1992).

[Bha96] S. S. Bhattacharyya, P. K. Murthy, and E. A. Lee, *Software Synthesis from Dataflow Graphs*, Kluwer Academic Publishers, Norwell MA, 1996. (`http://ptolemy.eecs.berkeley.edu/papers/96/softSynthBook/`)

[Bie90] J. Bier, E. Goei, W. Ho, P. Lapsley, M. O'Reilly, G. Sih and E.A. Lee, "Gabriel: A Design Environment for DSP," *IEEE Micro Magazine*, October 1990, vol. 10, no. 5, pp. 28-45.

[Bla92] Nancy Blachman, *Mathematica: A Practical Approach*, Prentice-Hall, ISBN 0-13-563826-7, 1992.

[Bol91] I. Bolsens, S. De Troch, L. Philips, B. Vanhoof, *et al.*, "Assessment of the Cathedral-II Silicon Compiler For Digital-Signal-Processing Applications," *ESA Journal*, vol. 15, no. 3-4, pp. 243-260, June 1991.

[Bro88] Randy Brown, "Calendar Queues: A Fast O(1) Priority Queue Implementation for the Simulation Event Set Problem," *Communications of the ACM*, vol. 31, no. 10, October 1988.

[Buc91] J. Buck, S. Ha, E. A. Lee, and D. G. Messerschmitt, "Multirate Signal Processing in Ptolemy," *Proc. of Int. Conf. on Acoustics, Speech, and Signal Process-*

ing, Toronto, Canada, April 1991, vol. 2, pp. 1245-1248.

[Buc93a] J. Buck and E. A. Lee, “The Token Flow Model,” *Advanced Topics in Dataflow Computing and Multithreading,* ed. L. Bic, G. Gao, and J. Gaudiot, IEEE Computer Society Press, 1993.

[Buc93b] J. T. Buck and E. A. Lee, “Scheduling Dynamic Dataflow Graphs with Bounded Memory Using the Token Flow Model,” *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, Minneapolis, MN, April 1993, vol. I, pp. 429-432.

[Buc93c] J. Buck, *Scheduling Dynamic Dataflow Graphs with Bounded Memory Using the Token Flow Model*, Ph. D. Dissertation, EECS Dept., UC Berkeley, Berkeley CA 94720, September 1993.

[Buc94] J. Buck, S. Ha, E. A. Lee, and D. G. Messerschmitt, “Ptolemy: A Framework for Simulating and Prototyping Heterogeneous Systems,” *Int. Journal of Computer Simulation*, special issue on “Simulation Software Development,” January 1994.

[Cha97] W.-T. Chang, S.-H. Ha, and E. A. Lee, “Heterogeneous Simulation -- Mixing Discrete-Event Models with Dataflow,” invited paper, RASSP special issue of the Journal on VLSI Signal Processing, January, 1997. (`http://ptolemy.eecs.berkeley.edu/papers/96/heterogeneity`)

[Che94] M. J. Chen, *Developing a Multidimensional Synchronous Dataflow Domain in Ptolemy*, MS Report, ERL Technical Report UCB/ERL No. 94/16, University of California, Berkeley, CA 94720, May 6, 1994.

[Den75] J. B. Dennis, *First Version Data Flow Procedure Language*, Technical Memo MAC TM61, May 1975, MIT Laboratory for Computer Science.

[Edw97] S. A. Edwards, *The Specification and Execution of Heterogeneous Synchronous Reactive Systems*, Ph. D. Dissertation, ERL Technical Report UCB/ERL M97/31, EECS Dept., University of California, Berkeley, 1997.(`http://ptolemy.eecs.berkeley.edu/papers/97/sedwardsThesis/`

[Eva93] B. L. Evans, *A Knowledge-Based Environment for the Design and Analysis of Multidimensional Multirate Signal Processing Algorithms,* Ph. D. Dissertation, School of Electrical Engineering, Georgia Institute of Technology, Atlanta, GA, June 1993.

[Eva95] B. L. Evans, S. X. Gu, A. Kalavade, and E. A. Lee, “Symbolic Computation in System Simulation and Design,” Invited Paper, *Proc. of SPIE Int. Sym. on Advanced Signal Processing Algorithms, Architectures, and Implementations*, July 9-16, 1995, San Diego, CA, pp. 396-407.

[Eva96] G. Arslan, B. L. Evans, F. A. Sakarya, and J. L. Pino, “Performance Evaluation and Real-Time Implementation of Subspace, Adaptive, and DFT Algorithms for Multi-Tone Detection,” *Proc. Int. Conf. on Telecommunications,* Istanbul, Turkey, April 15-17, 1996.

[Gen90] D. Genin, P. Hilfinger, J. Rabaey, C. Scheers, *et al.*, “DSP Specification Using the Silage Language,” *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1990, vol. 2, pp. 1056-60.

[Ha91] Soonhoi Ha and E.A. Lee, “Compile-Time Scheduling and Assignment of Dataflow Program Graphs with Data-Dependent Iteration,” *IEEE Trans. on Computers*, vol. 40, no. 11, pp. 1225-1238, November 1991.

[Ha92] S. Ha, *Compile-Time Scheduling of Dataflow Program Graphs with Dynamic Constructs*, Ph. D. Dissertation, EECS Dept., University of California, Berkeley, CA 94720, April 1992.

[Han96] Duane Hanselman and Bruce Littlefield, *Mastering MATLAB*, Prentice Hall, ISBN 0-13-191594-0, 542 pages, 1996.

[Har86] D. Harrison, P. Moore, R. Spickelmier, and A. R. Newton, ‘‘Data Management and Graphics Editing in the Berkeley Design Environment,’’ *Proc. of IEEE Int. Conf. on Computer-Aided Design*, November 1986, pp. 24-27.

[Has93] P. Haskell, *Flexibility in the Interactions Between High-Speed Networks and Communications Applications,* Ph. D. dissertation, EECS Dept., UC Berkeley, Berkeley CA 94720, October 1993.

[Hil85] P. Hilfinger, “A High-Level Language and Silicon Compiler for Digital Signal Processing,” *Proc. of Custom Integrated Circuits Conference*, May 1985, pp. 213-216.

[Hoa78] C. Hoare, “Communicating Sequential Processes,” *Communications of the ACM*, August 1978, vol. 21, no. 8, pp. 666-677.

[Hu61] T.C. Hu, “Parallel Sequencing and Assembly Line Problems,” *Operations Research*, vol. 9, no. 6, 1961, p. 841-848.

[Hyl97] C. Hylands, E. A. Lee, and H. J. Reekie, “The Tycho User Interface System,” to be presented at the 5th Annual Tcl/Tk Workshop ‘97, Boston, Massachusetts, July, 1997. (`http://ptolemy.eecs.berkeley.edu/papers/97/tcltk-97/`)

[Kah74] G. Kahn, “The Semantics of a Simple Language for Parallel Programming,” *Info. Proc.*, Stockholm, Sweden, August 1974, pp. 471-475.

[Kah77] G. Kahn and D. B. MacQueen, “Coroutines and Networks of Parallel Processes,” *Info. Proc.*, Toronto, Canada, August 1977, pp. 993-998.

[Kal91] A. Kalavade, *Hardware/Software Codesign Using Ptolemy - A Case Study*, M.S. Report, Electronics Research Laboratory, University of California, Berkeley, CA 94720, December 1991.

[Kal93] A. Kalavade, and E.A. Lee, “A Hardware/Software Codesign Methodology for DSP Applications,” *IEEE Design and Test of Computers*, vol. 10, no. 3, pp. 16-28, September 1993.

[Kal94] A. Kalavade and E. A. Lee, “Manifestations of Heterogeneity in Hardware/Software Codesign”, *Proc. of Design Automation Conference*, San Diego, CA, June 1994.

[Kal96] Asawaree Kalavade, *System Level Codesign of Mixed Hardware-Software Systems,* Tech. Report, UCB/ERL 95/88, Ph.D. Dissertation, Dept. of EECS, University of California, Berkeley, CA 94720, September 1995.

[Kar66] R. M. Karp and R. E. Miller, “Properties of a Model for Parallel Computations: Determinancy, Termination, Queueing,” *SIAM Journal*, vol. 14, pp. 1390-1411, November 1966.

[Khi94] K. P. Khiar and E. A. Lee, “Modeling Radar Systems using Hierarchical Dataflow,” *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, Detroit, MI, May 8-12, 1995, pp. 3259-3262.

[Lao94] A. Lao, *Heterogeneous Cell-Relay Network Simulation and Performance Analysis with Ptolemy*, M.S. Report, Electronics Research Laboratory, University of California, Berkeley, CA 94720, February 1994.

[Lap91] P. D. Lapsley, *Host Interface and Debugging of Dataflow DSP Systems*, M.S. Thesis, Electronics Research Laboratory, University of California, Berkeley, CA 94720, December 1991.

[Lee87a] E. A. Lee and D. G. Messerschmitt, “Static Scheduling of Synchronous Data Flow Programs for Digital Signal Processing,” *IEEE Trans. on Computers*, vol. 36, no. 1, pp. 24-35, January 1987.

[Lee87b] E. A. Lee and D. G. Messerschmitt, “Synchronous Data Flow,” *Proc. of the IEEE.*, vol. 75, no. 9, pp. 1235-1245, September 1987.

[Lee89] E. A. Lee, W.-H. Ho, E. Goei, J. Bier, and S. Bhattacharyya, “Gabriel: A Design Environment for DSP,” *IEEE Trans. on Acoustics, Speech, and Signal Processing*, vol. 37, no. 11, pp. 1751-1762, November 1989.

[Lee91a] E. A. Lee, “Consistency in Dataflow Graphs,” *IEEE Trans. on Parallel and Distributed Systems*, vol. 2, no. 2, pp. 223-235, April 1991.

[Lee91b] E. A. Lee and J. C. Bier, “Architectures for Statically Scheduled Dataflow,” reprinted in *Parallel Algorithms and Architectures for DSP Applications*, ed. M. A. Bayoumi, Kluwer Academic Publishers, Dordrecht, Netherlands, 1991, pp. 159-90.

[Lee92] E. A. Lee, “A Design Lab for Statistical Signal Processing,” *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, March, 1992, vol. 4, pp. 81-84, San Francisco, CA.

[Lee93a] E. A. Lee, “Multidimensional Streams Rooted in Dataflow,” *Proc. IFIP Working Conference on Architectures and Compilation Techniques for Fine and Medium-Grain Parallelism*, January 1993, pp. 295-306, Orlando, FL.

[Lee93b] E. A. Lee, “Representing and Exploiting Data Parallelism Using Multidimensional Dataflow Diagrams," *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1993, vol. I, pp. 453-456, Minneapolis, MN.

[Lee94] E. A. Lee, "Computing and Signal Processing: An Experimental Multidisciplinary Course," *Proc. of IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, vol. VI, pp. 45-48, Adelaide, Australia, April 1994.

[Lee95] E. A. Lee and T. M. Parks, "Dataflow Process Networks," *Proc. of the IEEE*, vol. 83, no. 5, pp. 773-801, May 1995 (`http://ptolemy.eecs.berkeley.edu/papers/processNets`).

[Lee96] E. A. Lee and A. Sangiovanni-Vincentelli, "The Tagged Signal Model -- A Preliminary Version of a Denotational Framework for Comparing Models of Computation," ERL Memorandum UCB/ERL M96/33, University of California, Berkeley, CA, 94720, June 4, 1996. (`http://ptolemy.eecs.berkeley.edu/papers/96/denotational/`).

[Mes84a] D. G. Messerschmitt, "A Tool for Structured Functional Simulation," *IEEE J. on Selected Areas in Communications*, vol. 2, no. 1, pp. 137-147, January, 1984.

[Mes84b] D. G. Messerschmitt, "Structured Interconnection of Simulation Programs," *Proc. of Globecom*, November 1984, vol. 2, pp. 808-811, Atlanta, Georgia.

[Mue93] F. Mueller, "A Library Implementation of POSIX Threads Under Unix," *USENIX Conference*, San Diego, CA, January 1993, pp. 29-41.

[Mue95] F. Mueller, "Pthreads Library Interface," Tech. Rep., July, 1995, available by `ftp://ftp.cs.fsu.edu/pub/PART/publications/pthreads_interface.ps.Z`.

[Mur93] P. K. Murthy, *Multiprocessor DSP Code Synthesis in Ptolemy*, Memorandum No. UCB/ERL M93/66, Electronics Research Laboratory, University of California, Berkeley CA 94720, 1993.

[Mur94a] P. K. Murthy, S. Bhattacharyya, and E. A. Lee, "Minimizing Memory Requirements For Chain-Structured Synchronous Dataflow Programs," *Proc. of IEEE Int. Conf. on Acoustics, Speech, and Signal Processing*, vol. II, pp. 453-456, Adelaide, Australia, April 1994.

[Mur94b] P. K. Murthy and E. A. Lee, "On the Optimal Blocking Factor for Blocked, Non-Overlapped Schedules," *Proc. of the IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, November 1994.

[Mur96] P. K. Murthy, "Scheduling Techniques for Synchronous and Multidimensional Synchronous Dataflow", Ph.D. Dissertation, Tech. Memo UCB/ERL M96/79, Dept. of EECS, Electronics Research Laboratory, Berkeley, Ca 94720, 1996. (`http://ptolemy.eecs.berkeley.edu/papers/96/murthyThesis/`).

[Not91] S. Note, W. Geurts, F. Catthoor, and H. De Man, "Cathedral-III: Architecture-

Driven High-Level Synthesis For High-Throughput DSP Applications," *Proc. of the 28th ACM/IEEE Design Automation Conference*, June 1991, pp. 597-602.

[Ous90] J. K. Ousterhout, "Tcl: An Embeddable Command Language," *Proc. of USENIX Conference*, January 1990, pp. 133-146.

[Ous91] J. K. Ousterhout, "An X11 Toolkit Based on the Tcl Language," *Proc. of USENIX Conference*, January 1991, pp. 105-115.

[Ous94] J. K. Ousterhout, *An Introduction to Tcl and Tk,* Addison-Wesley Publishing, Redwood City, CA, 1994, ISBN 0-201-63337-X.

[Par95] T. M. Parks, *Bounded Scheduling of Process Networks*, Technical Report UCB/ERL 95/105, Ph.D. Dissertation, EECS Department, University of California, Berkeley, CA, 94720-1770, December 1995. (http://ptolemy.eecs.berkeley.edu/papers/parksThesis/).

[Pin93] J. Pino, S. Ha, E. Lee, and J. Buck, "Software Synthesis for DSP Using Ptolemy," invited paper in the *J. on VLSI Signal Processing*, vol. 9, no. 1, pp. 7-21, January 1995.

[Pin94] J. L. Pino, T. Parks, and E. A. Lee, "Automatic Code Generation for Heterogeneous Multiprocessors," *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1994, vol. II, pp. 445-448, Adelaide, Australia.

[Pin95] J. L. Pino and E. A. Lee, "Hierarchical Static Scheduling of Dataflow Graphs onto Multiple Processors," *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, May 1995, pp. 2643-2646, Detroit, MI.

[Pin95] J. L. Pino, S. S. Bhattacharyya, and E. A. Lee, "*A Hierarchical Multiprocessor Scheduling Framework for Synchronous Dataflow Graphs*," *Proc. of the IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, October 29 - November 1, 1995.

[Pin96] J. L. Pino, T. Parks, and E. A. Lee, "Interface Synthesis in Heterogeneous System-Level DSP Design Tools," *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, May 1996, Atlanta, GA.

[Rab91] J. Rabaey, C. Chu, P. Hoang, and M. Potkonjak, "Fast Prototyping of Datapath-Intensive Architectures," *IEEE Design and Test of Computers*, vol. 8, no. 2, pp. 40-41, June 1991.

[Shi94] S.-I. Shih, *Code Generation for VSP Software Tool in Ptolemy*, MS Report, Plan II, ERL Technical Report UCB/ERL M94/41, University of California, Berkeley, CA 94720, May 25, 1994.

[Sih93a] G. C. Sih and E. A. Lee, "A Compile-Time Scheduling Heuristic for Interconnection-Constrained Heterogeneous Processor Architectures," *IEEE Trans. on Parallel and Distributed Systems,* vol. 4, no. 2, February 1993.

[Sih93b] G. C. Sih and E. A. Lee, "Declustering: A New Multiprocessor Scheduling

Technique," *IEEE Trans. on Parallel and Distributed Systems,* vol. 4, no. 6, pp. 625-637, June 1993.

[Sil91] *Silage User's and Reference Manual*, Prepared by Mentor Graphics/EDC, June, 1991.

[SS92] *Sproc Signal Processor Databook*, Star Semiconductor, 1992

[Sri93] S. Sriram and E. A. Lee, "Design and Implementation of an Ordered Memory Access Architecture," *Proc. of Int. Conf. on Acoustics, Speech, and Signal Processing*, April 1993, vol. I, pp. 345-348, Minneapolis, MN.

[Tho88] R. Alverson, *et al., THOR user's manual: Tutorial and commands,* Technical Report CSL-TR-88-348, Stanford University, January 1988.

[Vai92] P. P. Vaidyanathan, "Multirate Digital Filters, Filter Banks, Polyphase Networks, and Applications: A Tutorial," *Proc. of the IEEE*, vol. 78, no. 1, pp. 56-93, January 1990.

[Wal92] G. Walter, *ATM, Speech Coding, and Cell Recovery*, M.S. Report, EECS Dept., University of California, Berkeley, CA 94720, December 1992.

[Wel96] B. Welch, *Practical Programming in Tcl and Tk*, Prentice Hall, ISBN 0-13-182007-9, 1995.

[Whi93] K. White, *Xpole: An Interactive, Graphical Signal Analysis and Filter Design Tool*, Tech. Rep. M93/70, Electronics Research Laboratory, University of California, Berkeley, CA 94720, May 1993.

[Wol91] S. Wolfram, *Mathematica: A System for Doing Mathematics by Computer*, Addison-Wesley, ISBN 0-201-51502-4, 1991.

[Won92] Anthony Wong, *A Library of DSP Blocks and Applications for the Motorola DSP96000 Family*, M.S. Report, Plan II, EECS Dept., UC Berkeley, CA 94720, May 1992.