Embedded System Design for Wireless Applications

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Berkeley Wireless Research Center

The Distributed Approach to Information Processing

Source: Richard Newton

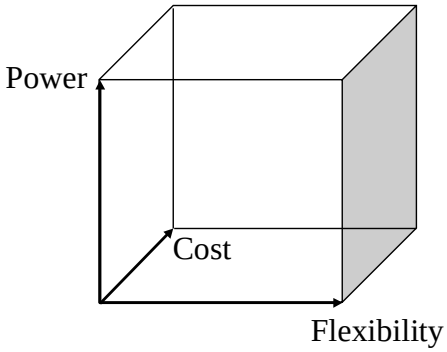
DAC System Le Design with Embedd Platforms Tutorial

The Wireless System Design Challenge

The Battery Limitation

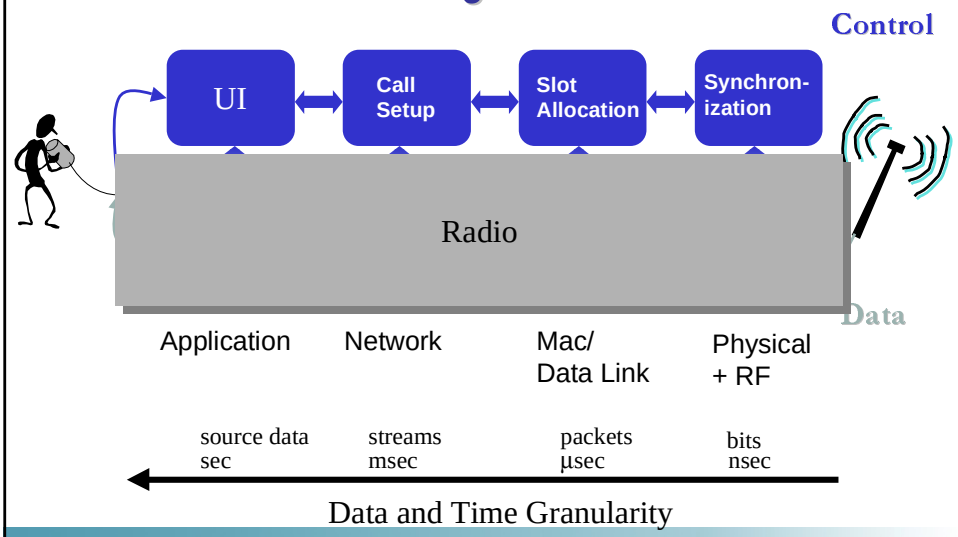
- **Projected energy per digital operation (2004): 50 pJ**
- **Lithium-Ion: 220 Watt-hours/kg == 800 Joules/gr**
- **At 50 pJ/operation:10 teraOps/gr!**
  - Equivalent to continuous operation at 100 MOPS for 30 hours (or average power dissipation of 6 mW)

The Changing Metrics

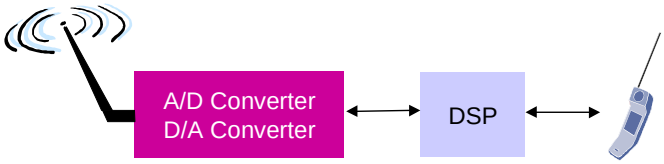


Performance as a Functionality Constraint
("Just-in-Time Computing")

The Wireless Challenge

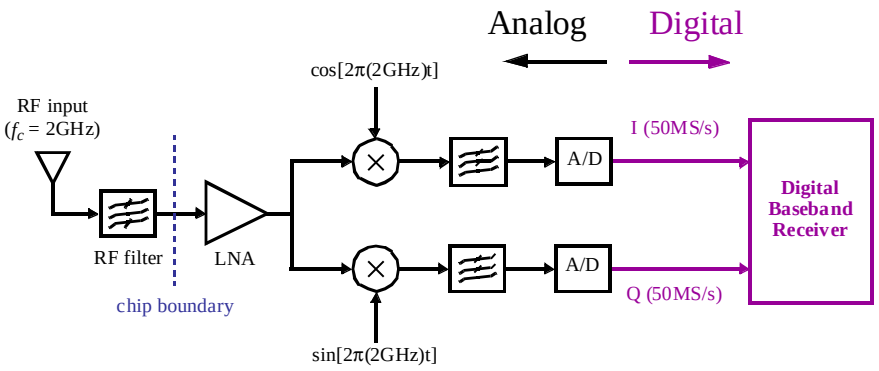


The Software Radio

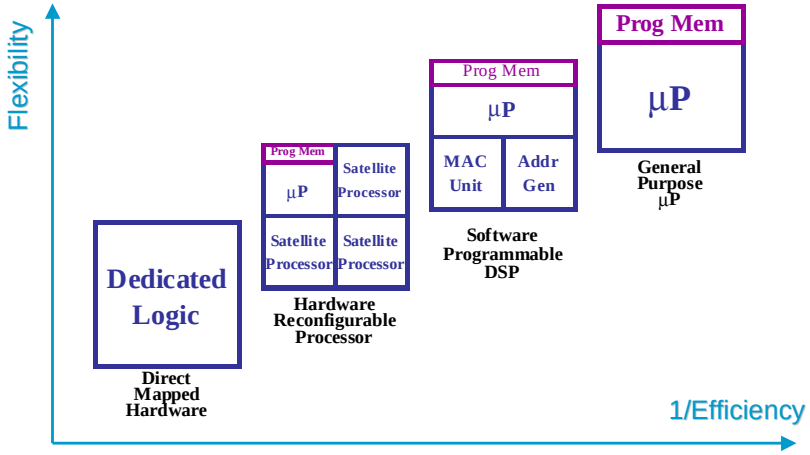


- **Idea: Digitize (wideband) signal at antenna and use signal processing to extract desired signal**
- **Leverages of advances in technology, circuit design, and signal processing**
- **Software solution enables flexibility and adaptivity, but at huge price in power and cost**
- **16 bit A/D converter at 2.2 GHz dissipates 1 to 10 W**

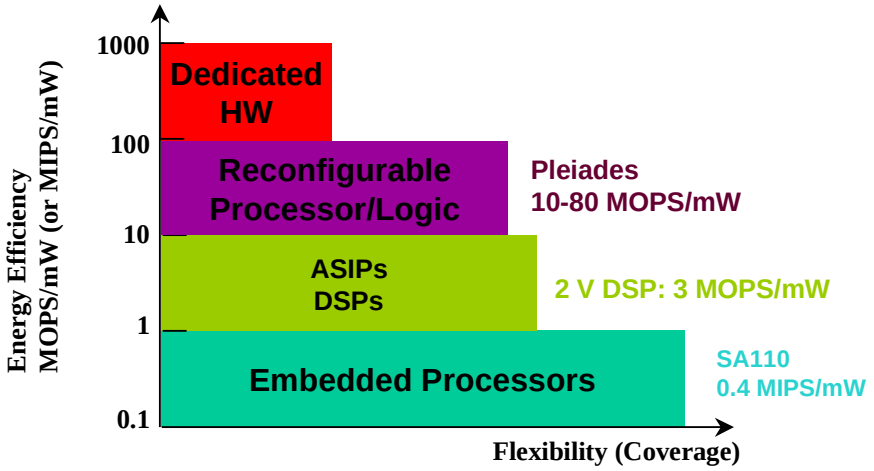
The Mostly Digital Radio



Architectural Choices



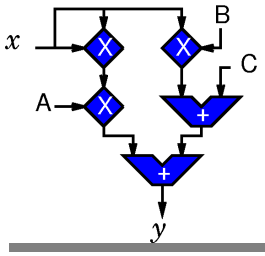
The Energy-Flexibility Gap



(Re)configurable Computing: Merging Efficiency and Versatility

Spatially programmed connection of processing elements.

$$y = Ax^2 + Bx + C$$



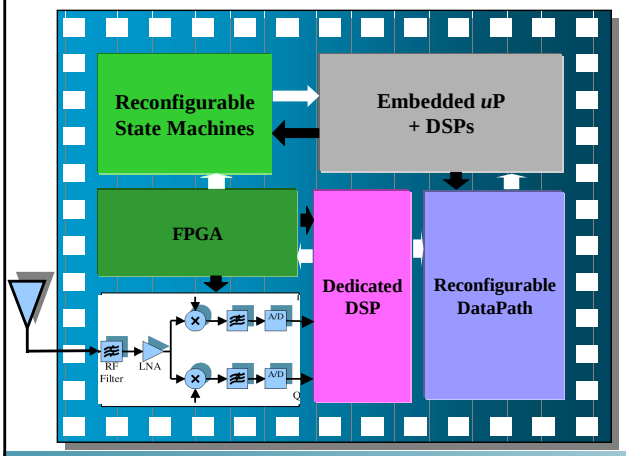
"Hardware" customized to specifics of problem.

- Direct map of problem specific dataflow, control.

Circuits "adapted" as problem requirements change.

The Implementation Opportunity

The Radio-on-a-Chip

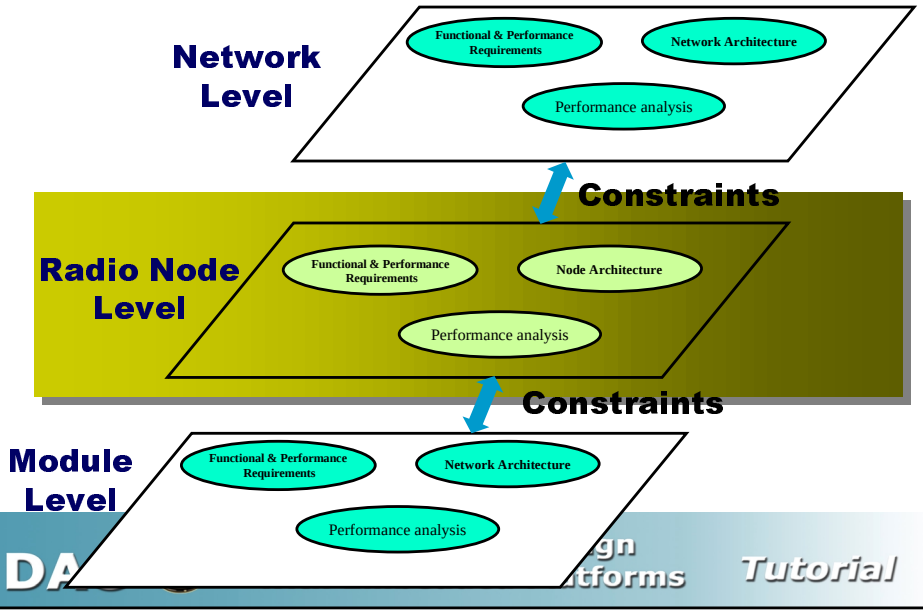


- DSP and control intensive
- Mixed-mode
- Combines programmable, flexible, and application-specific modules
- Cost and energy are the key metrics

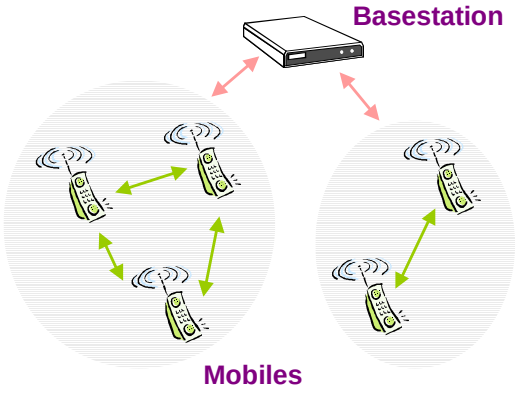
The Radio-on-a-Chip Design Problem

- **Multiple levels of design optimization**
  - The "fractal nature" of design
- **Capturing the functionality**
- **Capturing the architectural choices**
- **Quantifying the exploration trade-off's**

System Optimization Hierarchy



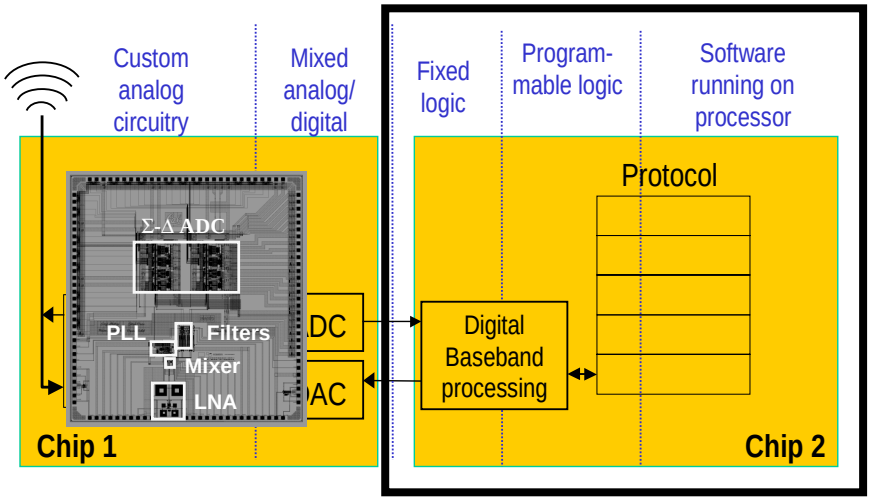
Digital Intercom — A Design Exercise in Communication/Component Based Design



- Known and tested specification of limited complexity allows focus on architectural implementation methodology
- Two-chip implementation leverages separates between analog (RF) and digital design concerns

Up to 20 users per cell @ 64 kbit/sec per link
TDMA selected as MAC protocol

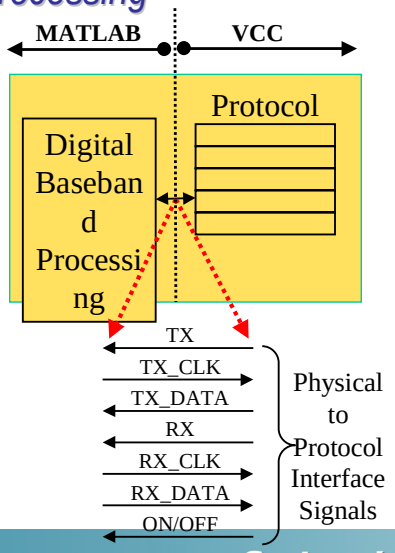
Two-Chip Intercom (TCI)



Direct down-conversion front-end (Yee et al)

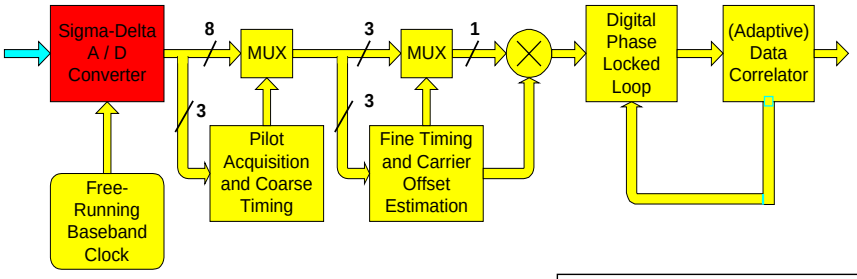
Our focus

Separation of Digital Communications and Protocol Processing

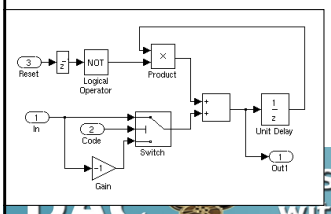


- Different tool environments require up-front partitioning
- Interface design critical to ensuring final designs work together
  - Small number of interface signals
  - Clearly specified behavior and constraints
- Verification relying on co-simulation

Digital Baseband (receiver)

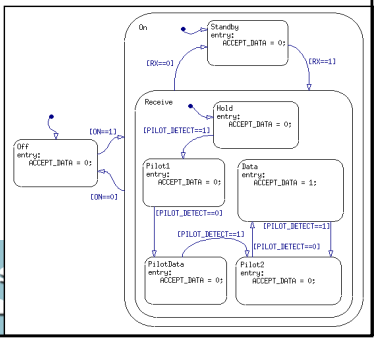


Functional Description:
Simulink + Stateflow (The Mathworks)

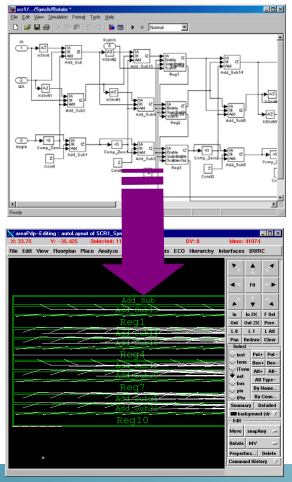


← Simulink example:
Matched filter correlator

Stateflow example: →
Receiver controller



Direct Mapping – an obvious choice for high-performance data-flow



Design Estimations (First order)
From Simulink Schematic:
RF + ADC/DAC
Transmit: 30 mW
Receive: 70 mW
Digital (conservative)
Transmit: 20 mW (100,000 transistors)
Receive: 80 mW (700,000 transistors)

UC Berkeley ICMake Flow (Brodersen)

Performance Analysis of Baseband Processing Produces Timing Constraints for Protocol Design

Estimates for the performance of the TCI Physical layer

	Rates		Duration	
	Hz	MHz	s	us
Chip	2.50E+07	25.00	4.00E-08	0.04
Symbol	8.06E+05	0.81	1.24E-06	1.24
Bit	1.61E+06	1.61	6.20E-07	0.62
				0.00
Pilot symbol			1.24E-06	1.24
Pilot sequence			1.86E-05	18.60

The transmit protocol will send a pilot sequence, some small number of dummy data bits (PD), another pilot sequence, and the real data bits (DAT) with the constraint that DAT<safe # sequential symbols

TX = PS | PD | PS | DAT

PD		0.0000124	12.40
DAT		0.004712	4712.00

time from RX to TX transition until :			
first DAT clock on transmitter	4.96E-05	49.60	(1)
time from TXCLK on Radio A until:			
RXCLK on radio B	2.58E-06		
time from TX on Radio A, and RX on radio B until:			
first DAT2 RXCLK on radio B	5.22E-05	52.18	(3)

Additional Calculations

Chips per Symbol	31
Bits per Symbol	2
Pilot sequence length	15
Channel coherency time	1.00E-01
BB clock coherency time (s)	5.00E-03
Max # sequential symbols (s)	4.03E+03
Safety margin	95.00%
Safe # sequential symbols	3.83E+03
PD (# of symbols)	10
DAT (# of symbols)	3800 OK

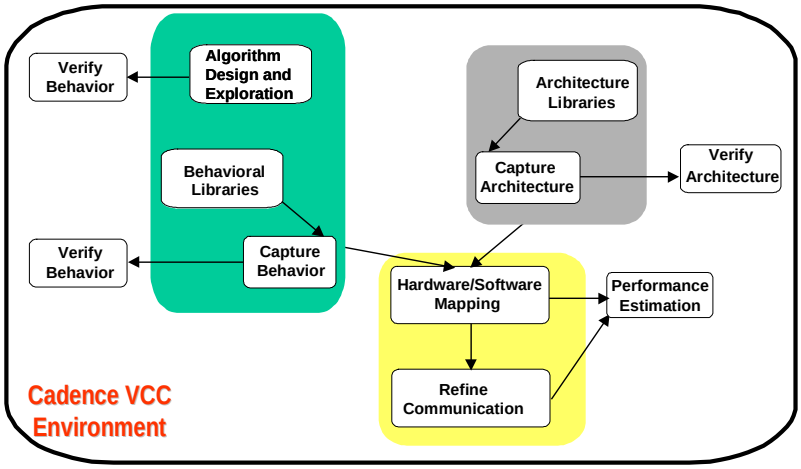
	meters	feet
Min distance	5	16.40
Max distance	10	32.81
		1
		1.00E+09

	s	us
	1.64E-08	0.02
	3.28E-08	0.03
Max time of flight (suggested by Paul bwo Dennis)	1.00E-07	0.10

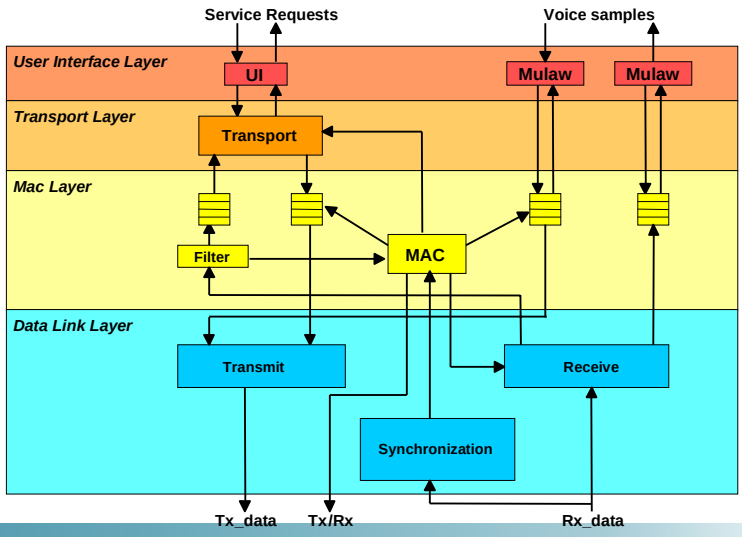
Tool: Microsoft Excel

Radio Turn-around Time

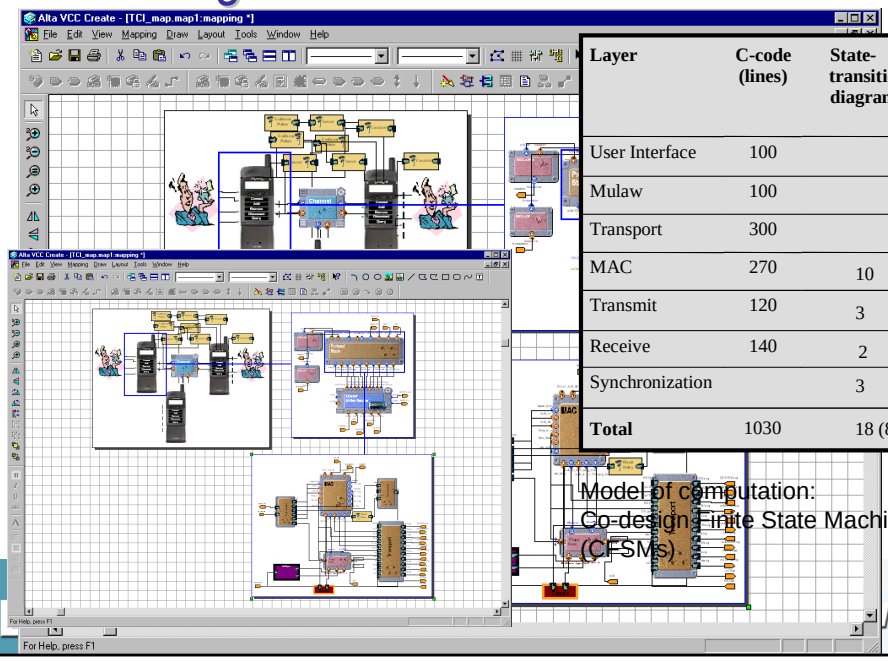
Exploring the Protocol Design Space



The Intercom Protocol Stack



Describing the Behavior



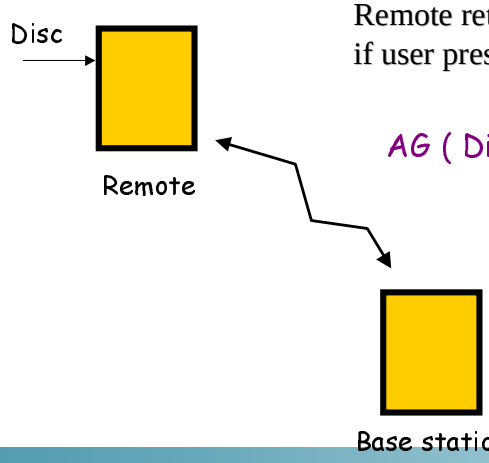
Layer	C-code (lines)	State-transition diagrams
User Interface	100	
Mulaw	100	
Transport	300	
MAC	270	10
Transmit	120	3
Receive	140	2
Synchronization		3
Total	1030	18 (80)

Model of computation:
Co-design Finite State Machines (CFSMs)

Formal Specification enables Verification

- **Does system satisfy certain properties?**
  - System described in some formal mathematical languages (e.g. Esterel, CFSM)
  - Properties written in some formal logic (e.g. Temporal Logic) or formal model (e.g. Esterel, CFSM)
- **Two approaches**
  - Property Verification
    - Invariant (only one remote can send voice data in any time slot)
    - Response (if a remote sends a request to the base station, then eventually there is an acknowledgement)
    - deadlock freedom
  - Refinement Checking
    - Does the (low-level) implementation conform with the (high-level) specification?
      (Do the mapped CFSMs function the same as the specification?)
- **Example: Mocha System (Henzinger, UCB)**

Example of Property Verification



Remote returns to the disconnect state if user presses the disconnect button.

AG (Disc→ AF (Not Conn))

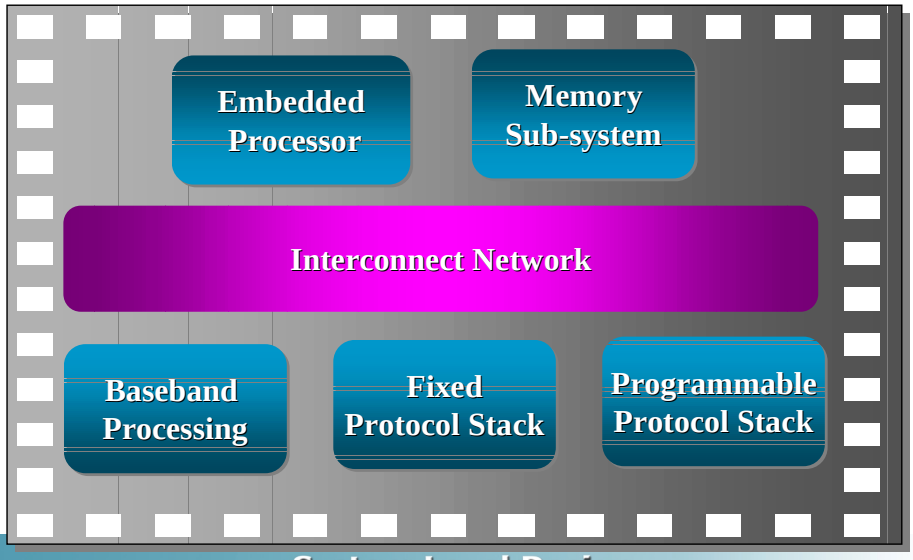
✖NOT OK

Why it Fails?

- Remote accepts *Disc* from the user even if it is not connected
- After the remote has sent *DiscReq* and waits for acknowledgement
- However, base station ignores *DiscReq* if remote is not registered

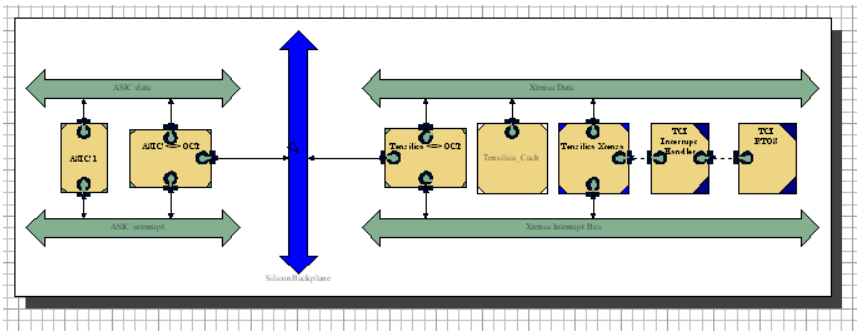
➔ Deadlock!

Targeted Implementation Platform



DAC System Level Design with Embedded Platforms Tutorial

The Architecture Description in VCC



Modeling the Architectural Components
The embedded processor

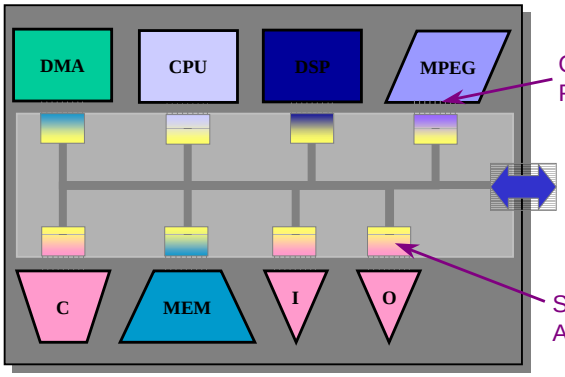
- **Xtensa embedded CPU (Tensilica, Inc)**
  - Configurability allows designer to keep "minimal" hardware overhead
  - ISA (compatible with 32 bit RISC) can be extended for software optimizations
  - Fully synthesizable
  - Complete HW/SW suite
- **VCC modeling for exploration**
  - Requires mapping of "fuzzy" instructions of VCC processor model to real ISA
  - Requires multiple models depending on memory configuration
  - ISS simulation to validate accuracy of model

◆ **Tensilica model in VCC**

The "fuzzy" instruction set

```
inst,LD,2          inst,MUL.c,9       inst,DIV.i,118
inst,LI,1          inst,MUL.s,10      inst,DIV.l,122
inst,ST,2          inst,MUL.i,18      inst,DIV.f,145
inst,OP.c,2        inst,MUL.l,22      inst,DIV.d,155
inst,OP.s,3        inst,MUL.f,45      inst,IF,5
inst,OP.i,1        inst,MUL.d,55      inst,GOTO,2
inst,OP.l,1        inst,DIV.c,19      inst,SUB,19
inst,OP.f,1        inst,DIV.s,110     inst,RET,21
inst,OP.d,6
```

Modeling the Architectural Components
The Interconnect Network

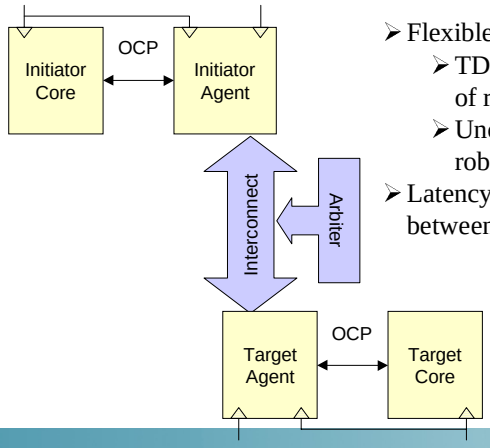


Guaranteed Bandwidth Arbitration

"The Silicon Backplane" (Sonics, Inc)

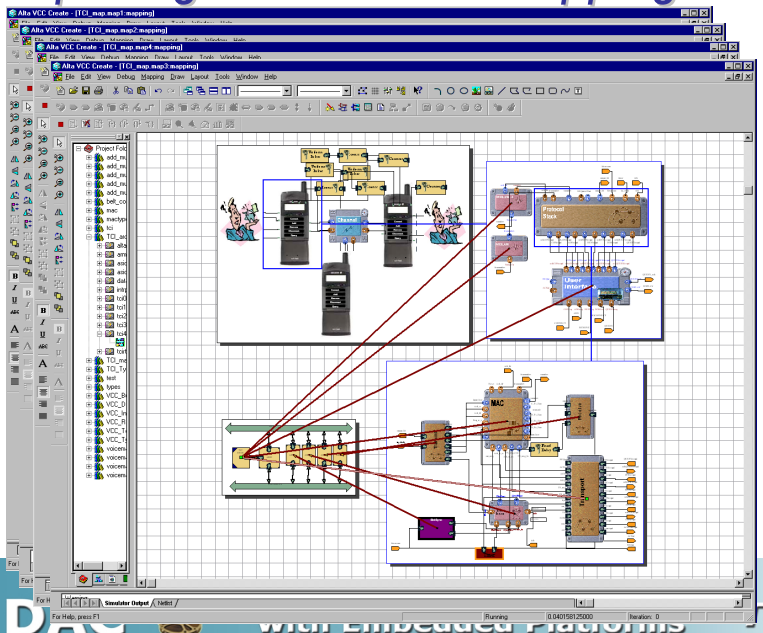
Modeling the Architectural Components
The Interconnect Network

- **"Silicon Backplane" model in VCC**



- Flexible bandwidth arbitration model
  - TDMA slot map gives slot owner right of refusal
  - Unowned/unused slots fall to round-robin arbitration
- Latency after slice granted is user-specified between 2-7 Bus Clock cycles

Exploring Architectural Mappings



Software Processor

Application

Transport

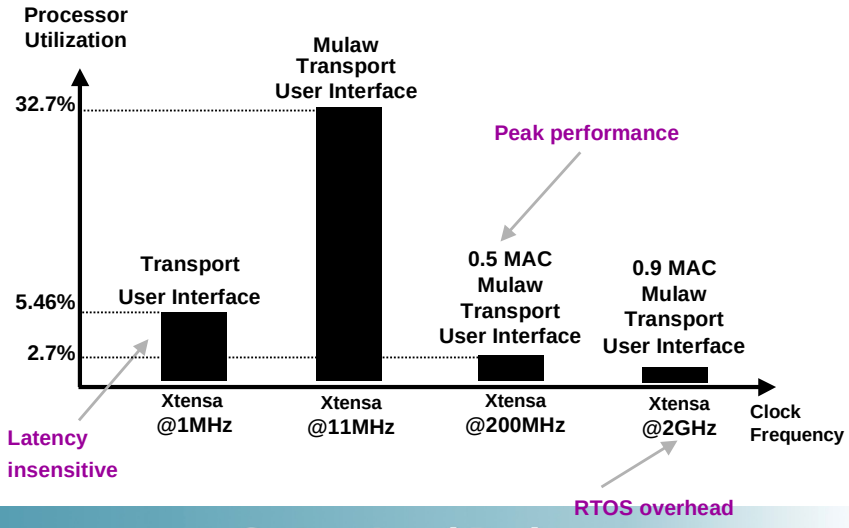
Mu-law

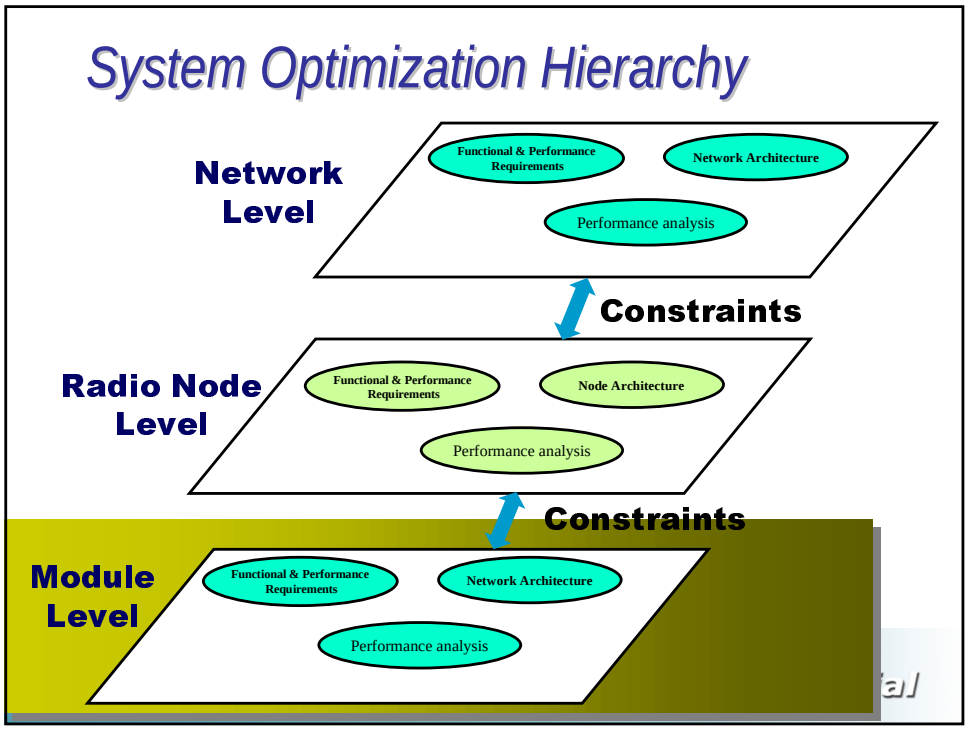
MAC

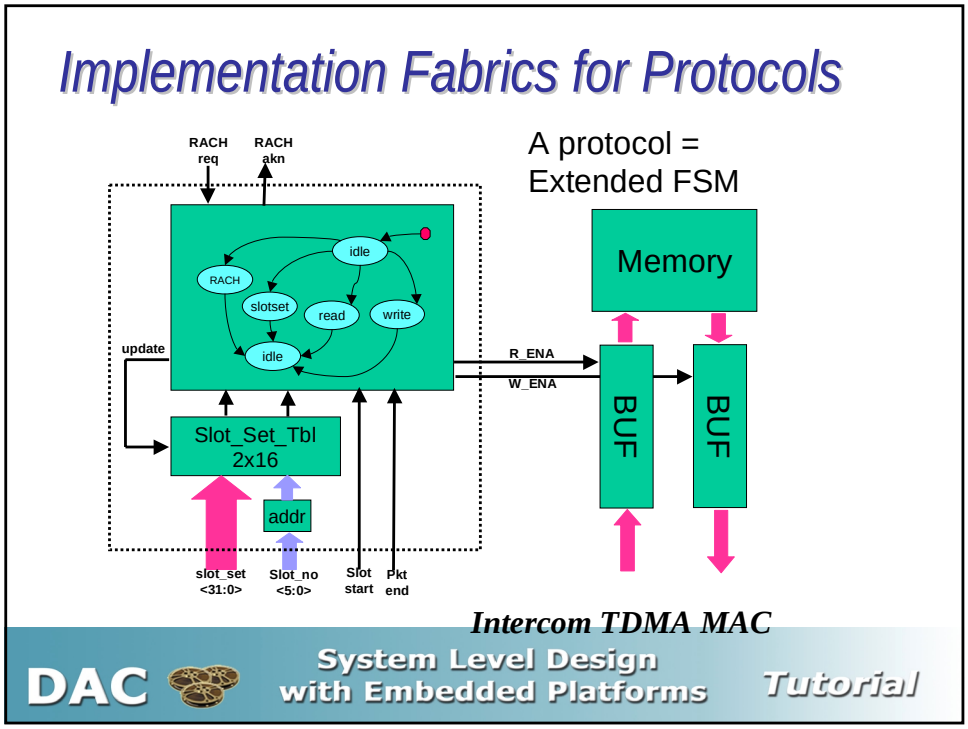
ASIC Accelerators

Rest

Processor Utilization - Estimation




System Optimization Hierarchy
Network Level
Functional & Performance Requirements
Network Architecture
Performance analysis
Constraints
Radio Node Level
Functional & Performance Requirements
Node Architecture
Performance analysis
Constraints
Module Level
Functional & Performance Requirements
Network Architecture
Performance analysis


Implementation Fabrics for Protocols
RACH req
RACH akn
A protocol = Extended FSM
idle
RACH
slotset
read
write
idle
update
Slot_Set_Tbl 2x16
addr
slot_set <31:0>
Slot_no <5:0>
Slot start
Pkt end
R_ENA
W_ENA
Memory
BUF
BUF
Intercom TDMA MAC
DAC
System Level Design with Embedded Platforms
Tutorial

Intercom TDMA MAC Implementation alternatives

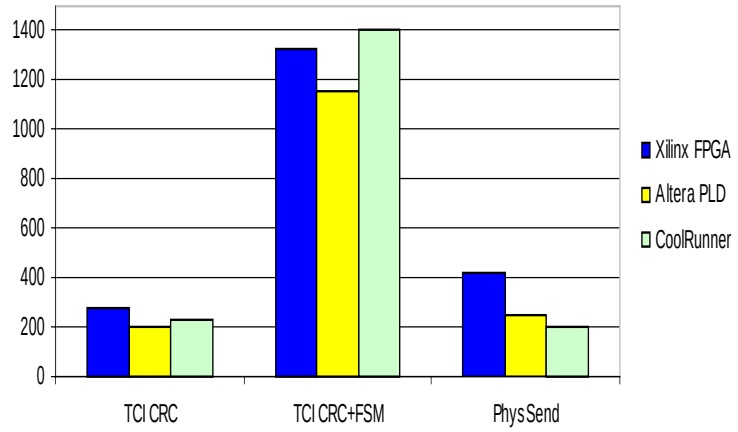
	ASIC	FPGA	ARM8
Power	0.26mW	2.1mW	*114mW*
Energy	10.2pJ/op	81.4pJ/op	*n*457pJ/op*

ASIC: 1V, 0.25 µm CMOS process
FPGA: 1.5 V 0.25 µm CMOS low-energy FPGA
ARM8: 1 V 25 MHz processor; n = 13,000
Ratio: 1 - 8 - >> 400

How much flexibility is really needed?

HW Mapping Experiment: Flexible Inplementation

Area Comparison - FPGA x PLD (Manual)



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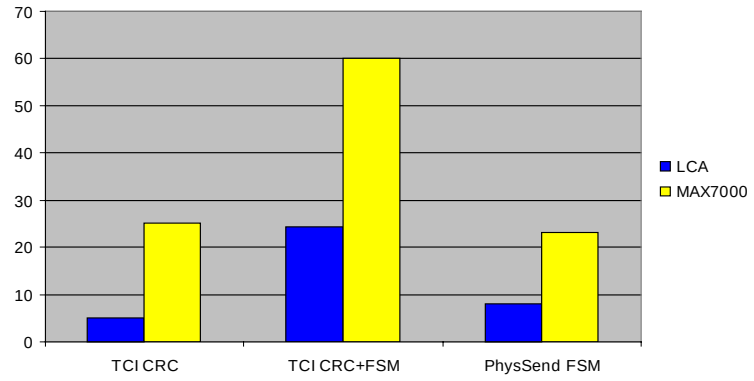
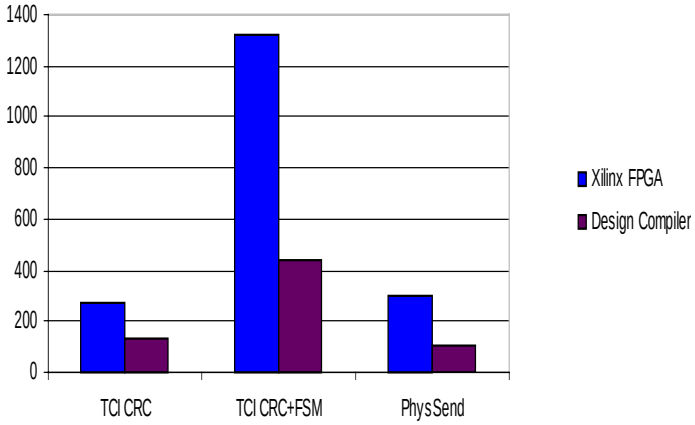
HW Mapping Experiment: Power Consumption

FPGA versus PLD



HW Mapping Experiment: Flexible versus Fixed

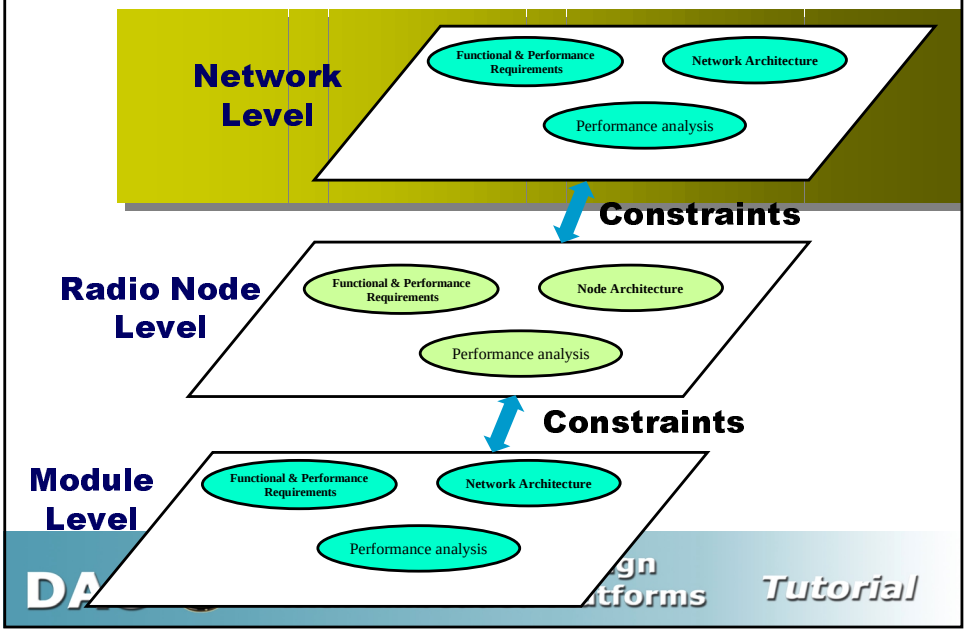
Area Comparison – FPGA x Std.Cell (Manual)



TCI Exploration Summary

- **Exploration at chip micro-architecture level enables dramatic improvements in various metrics – results often non-intuitive**
- **Obtaining this insight using other techniques is either extremely time-consuming, or naïve.**
- **Exploration tools such as VCC require a re-schooling of the designer – new abstractions at function and architecture level, new perspective on "accuracy" of predictions**
  - Yet learning curve is quite flat
  - Took graduate students approximately 1 month to get **fully** experienced with tools
  - Once descriptions and models are available, multiple options can be explored in a single day

The Fractal Nature of Design (again)



Picoradio's: Wireless Networks of Ubiquitous Sensors and Monitors

Example -The Smart Home and Network Appliances

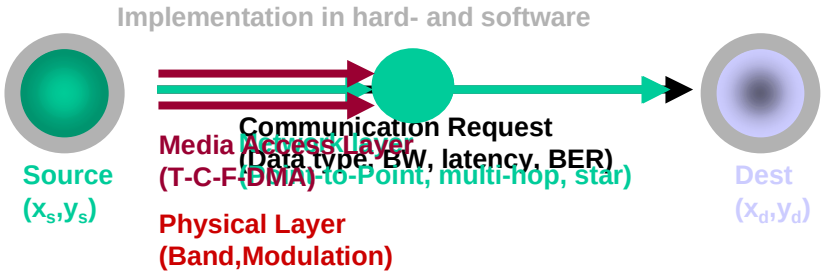
Other applications:
Office buildings, toys,
Interactive musea

Security
Environment monitoring and control
Object tagging
Identification

System Requirements and Constraints

- **Large numbers of nodes — between 0.05 and 1 nodes/m^2**
- **Cheap (<0.5$) and small (< 1 cm^3) and ultra low-power (< 100 μW) enabling energy scavenging**
- **Limited operation range of network — maximum 50-100 m**
- **Low data rates per node — 1-10 bits/sec average**
  - up to 10 kbit/sec in rare local connections to potentially support non-latency critical voice channel
- **Crucial Design Parameter:**
  Spatial capacity (or density) — 100-200 bits/sec/m^2

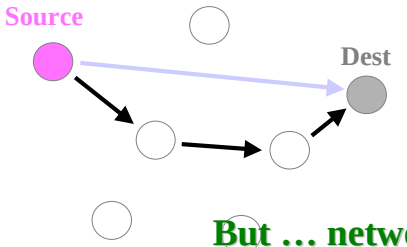
Wireless Communication Design Space Exploration



- **Step-wise refinement (partitioning, resource mapping and sharing) enables optimization, cost analysis, and correctness verification**
- **Based on well-defined abstraction layers**

Communicating over Long Distances

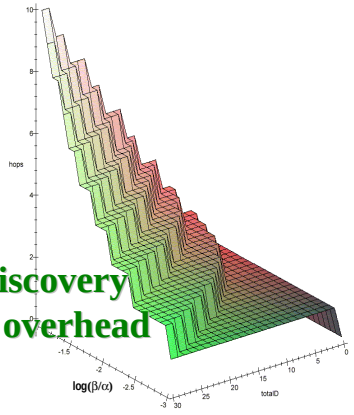
Multi-hop Networks



Example:

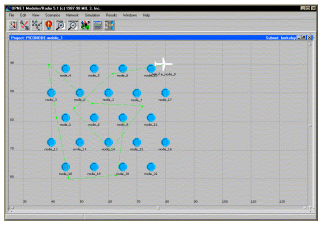
- **1 hop over 50 m**
  1.25 nJ/bit
- **5 hops of 10 m each**
  5 × 2 pJ/bit = 10 pJ/bit
- **Multi-hop reduces transmission energy by 125!**
  (assuming path loss exponent of 4)

But … network discovery and maintenance overhead

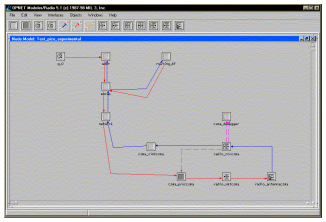


Optimal number of hops needed for free space path loss.

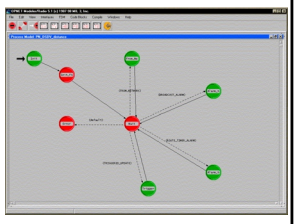
Network Model



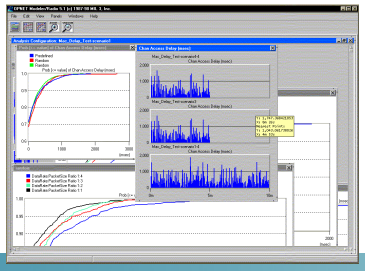
Node Model



Process Model



Analysis Viewer

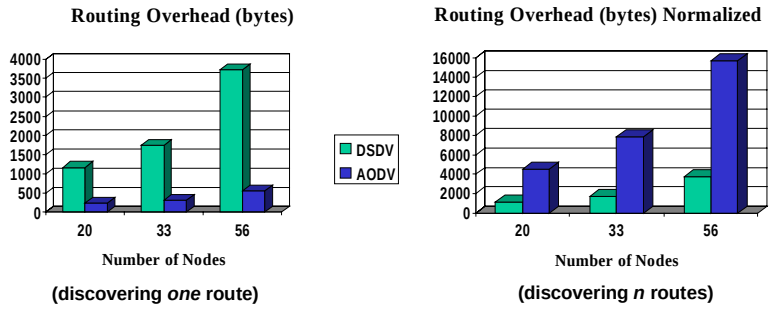


Network simulators combine functional models with cost model for computation and communication

OPNET
Network Simulator

Comparing Energy Cost of Networking Approaches

- **Energy = Eb * Packet Size**
- **Reactive Routing good for rarely used routes**
- **Proactive Routing good for frequently used routes**



(discovering *one* route)

(discovering *n* routes)

Summary

- Low-energy design ascends to prime time
  forced mainly by the last-meter problem
- System-on-a-Chip approach enables and demands heterogeneous implementation strategies, sometimes involving non-intuitive and innovative design platforms
- Design exploration over various fabrics and partitions has dramatic impact on dominant metrics, such as energy and cost
- It requires orthogonalization of function and architecture, supplemented with performance models (cost, time, energy)
  - Architectural models for exploration in high demand
- This methodology holds at all levels of the system hierarchy
  The Fractal Nature of Design