CSEE W3827

Fundamentals of Computer Systems

Homework Assignment 2

Solutions

Profs. Stephen A. Edwards & Martha Kim

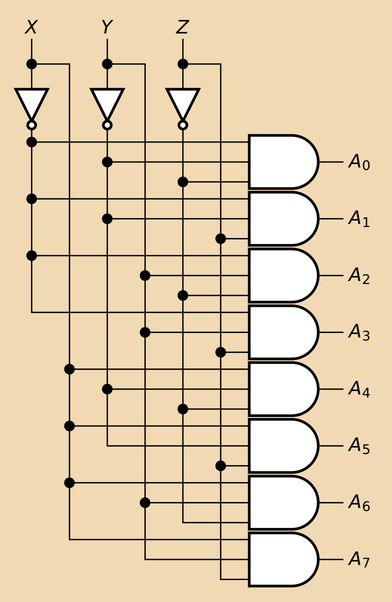
Columbia University

Due February 15th, 2012 at 1:10 PM

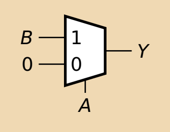
Include your name, UNI, and the names of any collaborators.

Show your work for each problem; we are more interested in how you get the answer than whether you get the right answer.

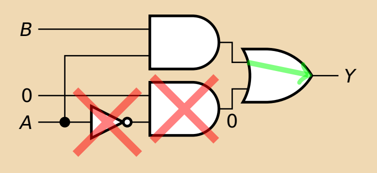
1. (10 pts.) Draw the circuit for a 3-to-8 decoder using AND gates and inverters. It should have three inputs X, Y, and Z and eight outputs, $A_0, \ldots, A_7$. Only one of the outputs should ever be true.



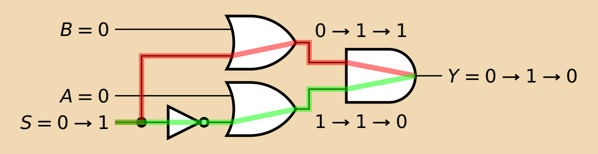
2. (a) (10 pts.) Show how to implement an AND gate using just a two-input mux and constant inputs (no additional gates).



(b) Show that when the mux2 is implemented as shown below, your solution simplifies to a single AND gate.

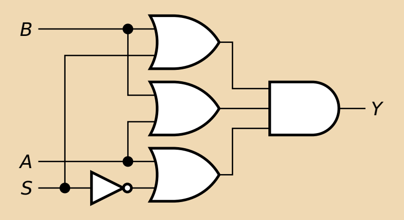


3. (20 pts.) Consider the following circuit.



(a) Under what conditions could the output of this circuit glitch high? I.e., for what assignment of input values would changing one input's value cause the output to briefly transition from 0 to 1 to 0?

(b) Modify this circuit (e.g., add or change gates and wires) so it computes the same function but cannot glitch in this situation.

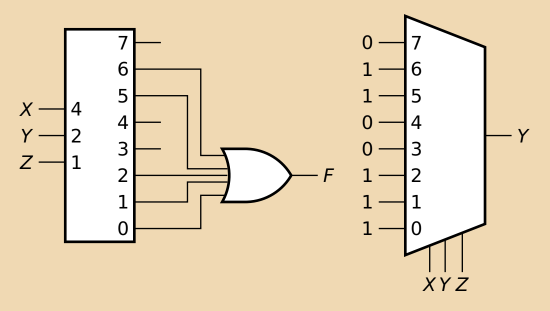


		A	A	
	0	0	1	1
S	0	1	1	0
			B	B

4. (15 pts.) Show how to implement $F = X\overline{Y}Z + Y\overline{Z} + \overline{X}\,\overline{Y}$ using

(a) a 3-to-8 decoder and an OR gate;

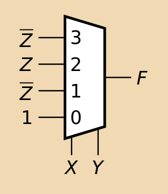
X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



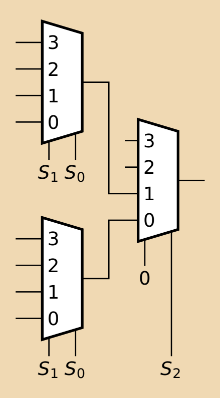
(b) an 8 input mux; and

(c) a 4 input mux whose select inputs are X and Y and an inverter.

X	Y	F
0	0	1
0	1	$\overline{Z}$
1	0	Z
1	1	$\overline{Z}$



5. (10 pts.) Draw a circuit for an eight-input mux using three four-input muxes and no other gates.



6. (35 pts.) Implement a three-bit binary carry-lookahead adder. Its inputs are $A_0, \ldots, A_2$ and $B_0, \ldots, B_2$ for the two addends and C_0 as the carry in. Its outputs are $Y_0, \ldots, Y_3$.

   (a) Write expressions for $G_0, \ldots, G_2$ and $P_0, \ldots, P_2$, the carry generate and propagate functions, in terms of the inputs.

   $G_0 = A_0 B_0$, $G_1 = A_1 B_1$, & $G_2 = A_2 B_2$.

   $P_0 = A_0 + B_0$, $P_1 = A_1 + B_1$, & $P_2 = A_2 + B_2$.

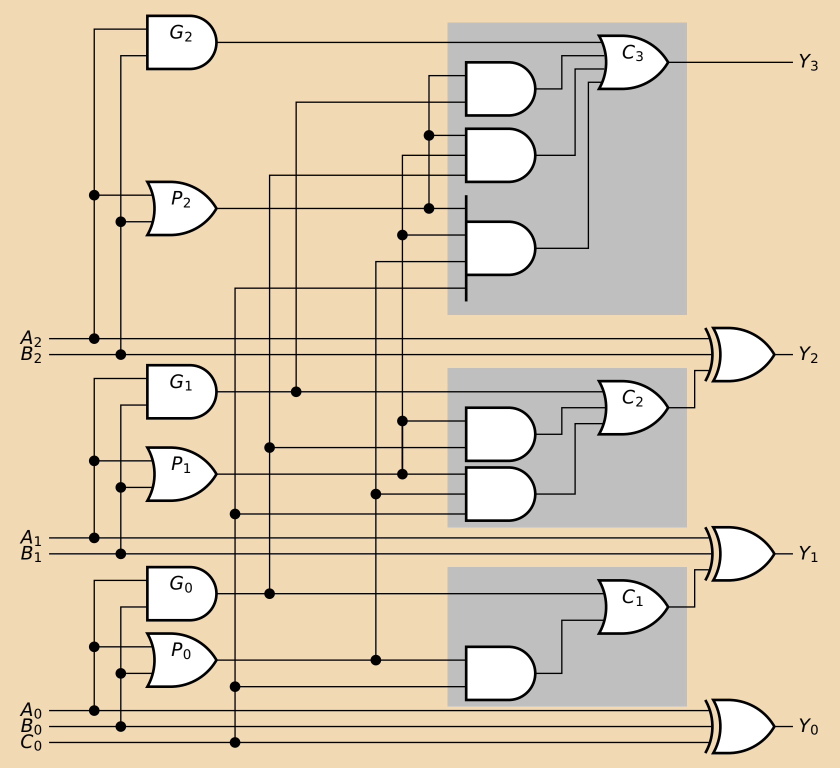
   (b) Write sum-of-product expressions for $C_1, \ldots, C_3$ in terms of the G's, P's, and C_0

   $C_1 = G_0 + C_0 P_0$
   $C_2 = G_1 + G_0 P_1 + C_0 P_0 P_1$
   $C_3 = G_2 + G_1 P_2 + G_0 P_1 P_2 + C_0 P_0 P_1 P_2$

   (c) Use these to write equations for the Y's (use "$\oplus$" for XOR).

   $Y_0 = A_0 \oplus B_0 \oplus C_0$
   $Y_1 = A_1 \oplus B_1 \oplus C_1$
   $Y_2 = A_2 \oplus B_2 \oplus C_2$
   $Y_3 = C_3$

   (d) Draw the carry-lookahead adder circuit corresponding to these equations using inverters, AND, NAND, OR, NOR, and XOR gates with as many inputs as you'd like. The critical path should be four gates. Please try to make your drawing neat.



G_2
C_3
Y_3
P_2
A_2
B_2
Y_2
G_1
C_2
P_1
A_1
B_1
Y_1
G_0
C_1
P_0
A_0
B_0
C_0
Y_0