CS W4840 Project Proposal

Anthony Erlinger (afe2104)
Jaebin Choi (jc3797)
Yu Chen (yc2615)
Arthy (as4304)

Team Name: *Double-O 4*

IP Synth: Producing audio from network data on the 4004

Abstract
IP Synth is an architecture for filtering raw network data from an emulation of the Intel 4004 CPU into an audible signal. This project will consist of three major milestones as follows.

The **first milestone** will be designing a VHDL version of the 4004 itself. Given its prominent history, there is a wealth of data available regarding the implementation of the 4004. We intend to reproduce the chip in VHDL by studying both its microarchitecture and physical layout and as well as its “black box” instruction set architecture.

The **second milestone** will involve interfacing the 4004 with the Altera’s network interface and processing the incoming hardware stream at a very low level. We will also run extensive tests on our implementation to be sure that we can process the incoming network data in a meaningful way.

Our **third milestone** is the most difficult will involve the processing the incoming data with the 4004. Given the high bandwidth of the input, some additional hardware may be necessary to downsample the incoming data at a reasonable throughput for the 4004. It is also reasonable to assume that much of the input will be pseudo-random. Therefore, we will perform basic operations on the data to make it more “palatable” to the human ear. Toward this end, basic instructions running within the CPU itself will process the incoming data stream to perform basic filtering operations (delay, modulation, volume, and so on) followed by piping the processed data to the sound card.

The team’s decision to pursue this project was chosen over other competing ideas based on its broad utilization of key technologies. Processing network data, designing a basic CPU, and filtering audio data are all interesting subject matters in their own right and also cater to the skillsets of our team. Still, uncertainties remain over running instructions over the virtual implementation of the 4004 (although we are considering other reduced ISA CPUs such as the z80 or Intel 8008), and we welcome any feedback.

Thanks,
- Team *Double-O 4*

Specific Objectives:

Hardware RTL Design:

1. Retrieve raw data from network card on Altera DE2 and store in RAM.
2. Design a basic CPU architecture to process data from the network card (4004).
3. Ensure CPU architecture is fully compatible with compiled code from NiOS

Software Design:

1. Fetch NIC data from RAM.
2. Run a closed loop running in a regular interval that:
    a. Fetches data from RAM
    b. Basic processing (Type)
    c. Send data to output device (Audio or Video)

Questions:

1. Input data bandwidth?
2. Feasibility of instruction execution on the 4004
3. Upstream vs. downstream network data