

Ah-Ah-Piu

Spring 2013 CSEE 4840 Embedded System Design

Final Project Report

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Overview

Ah-Ah-Piu is a platform shooting video game, which is uniquely controlled by voice. By and large, the game runs as follows. Players decide to make a sound or not, then this input will control the movement of the avatar in the game that thriving to advance and earn more points.

Before diving into the technical details, let's learn about the fascinating background story of Ah-Ah-Piu. The hero in our game is modeled from one of the co-designer, who is clearly having a good time taking the CSEE4840 course. Every lovely Tuesday and Thursday afternoon, he routinely comes to 1235 Mudd and tries whatever he can to avoid being terminated by all the dues and, of course, our be-loved Prof. Edwards. Hopefully, he can manage to get a perfect score in the end.

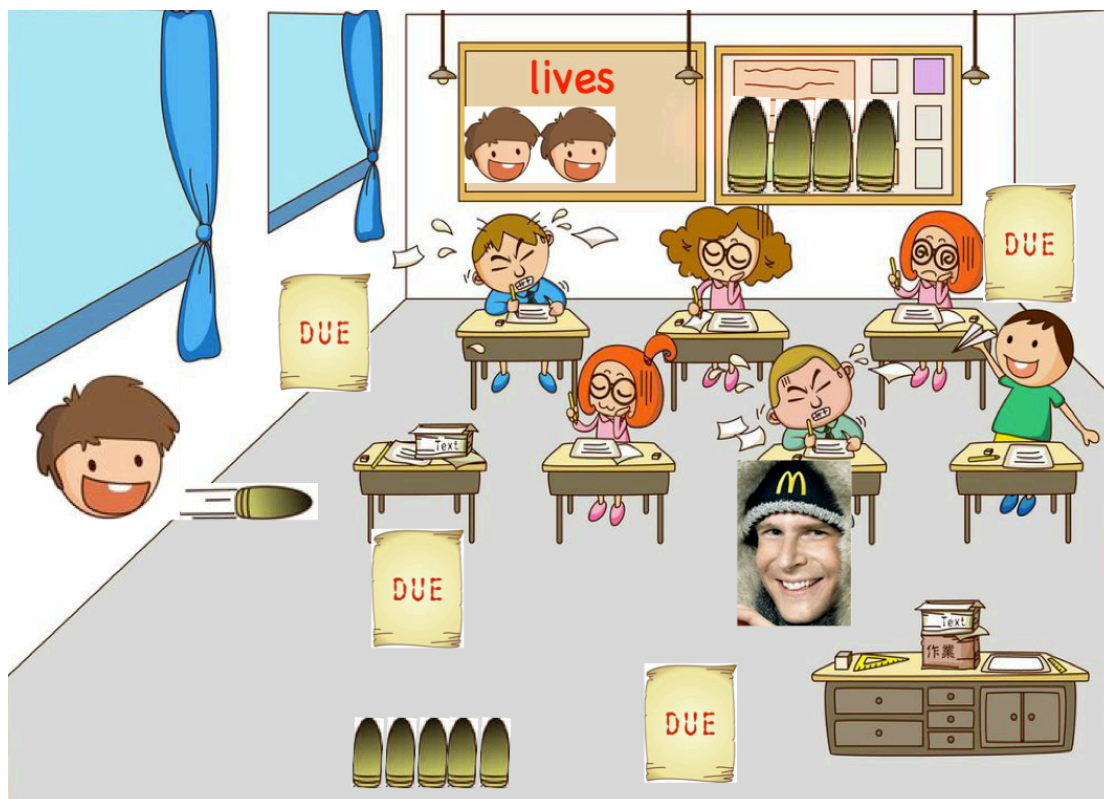


Figure1 Game View

Now let's walk through the game flow of Ah-Ah-Piu. When it is started, a starting view will be shown and if you make a sound now, the game will be activated. At the moment it is on, the dues will be randomly generated and appeared from the right edge of the screen moving towards the left side along a straight lane. The hero can move up and down along the left edge, controlled by the audio input. If you make a sound with long duration (not necessary to be "Ah"), the avatar will rise up, if you shout louder, the up-going speed will also increase, until he reach the top of the screen. Otherwise, if a short sound is detected (not necessarily to be "Piu"), the avatar will fire a bullet that goes along a straight line across the screen destroying the enemies on the way. However, you may want to use your bullets wisely since there is a bullet count appearing on the right blackboard up ahead, you can only have five rounds in one clip, but don't worry, there will be ammo supplies flying towards you together with the dues, you just have to shot or collide with them to get a refill of your weapon. If you keep silence, then the avatar will drop along the left edge in a predefined speed, until he touch the bottom.

Our game is set up in rounds that each one will keep on for 50 seconds. Of course, each round will be tougher then the last one, because the dues and the boss will move faster to attack you. The boss will appear every round to take you out showing no mercy at all. He is so powerful that you cannot take him out only if you can hit him 5 times in a row.

Our game is well defined in a sense that we have a comprehensive points calculating mechanism. The moment after the game is activated, there is a basic 2 points you can earn every seconds you stay in the game. By staying in the game it means you still have lives showing on the left blackboard up ahead. Initially, you have three lives to start with, every collision with the dues or Prof. Stephen, will cause you one life until you are swept out. To protect you not to be killed out so easily, we implement a safe mode in the following 5 seconds every time you lost a life. Besides the basic income, you can gain extra points by shooting and hitting. The points you currently have will be displayed on the screen. To make it more interesting, it will also be displayed by the LEDs on the DE2 board. When you are killed, a game-over view will appear and show what final score you got. We set up an algorithm to translate the number score to a letter manner. If you played well enough and get more then 200 points, you will get an A in the end.

Design

This section describes both the hardware and software design of our project. It starts by showing the high-level architecture of our design, then presents in details about our implementation in the order of hardware and software. For the hardware part, we further categorized it into three sub-sections, which are audio, VGA display, and memory allocation.

1. Architecture

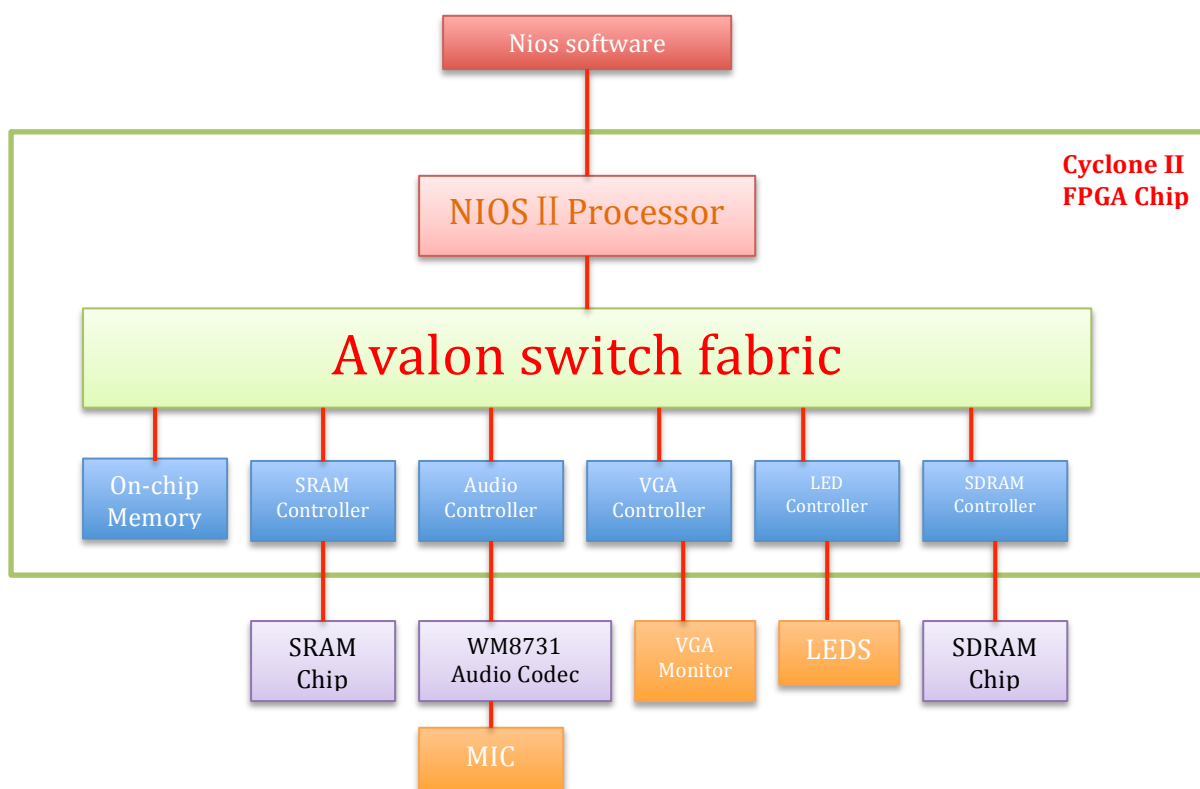


Figure 2 the design Architecture

Given above is the design architecture of our project. As you can see, the audio controller and VGA controller are the two most important pieces. The audio controller takes the responsibility to write the digital data coming out of the Audio Codec onto the Avalone bus. The VGA controller is in charge of reading data from the bus and using these data to paint the VGA monitor. What the software need to do is to read data from the Avalone bus to realize the sound control functionality, also takes care of the game logic such as enemy generation, collision detection and points calculation, then write data

back to the bus to instruct the VGA controller to paint the screen.

2. Implementation

2.1 Hardware

Since the Ah-Ah-Piu is a reasonably complete and well-rounded game, we have done a lot implementing on the hardware to achieve the desired functionality. As according to the class requirement, we balanced the work load between hardware and software, and try our best to do more on the hardware part.

The hardware of our project mainly includes three parts: the Audio, the VGA display, and the memory. The Audio part takes care the input from the mic as well as the sound effect outputted to the earphone; The VGA display make sure our game view is shown on the monitor properly; Since our game is well-formed and provide high quality visual experience, we have to take the challenge and provide enough memory resources to store all the game elements.

2.1.1 Audio

The audio plays a major role in our hardware design. Different from other keyboard or mouse controlled video games, the Ah-Ah-Piu requires instant ADC conversion so that we can utilized the digital output converted from the player's voice to control the game. Besides, in order to enrich our game experience, we add up various sounds effect and background music which output from the headphones. All these works are carried out by the Wolfson WM8731 Audio Codec.

Wolfson WM8731 Audio Codec

WM8731 is a low power stereo CODECs with an intergrated headphone driver. Both stereo line and mono microphone level audio input are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret type microphone. Besides, there also bulit in ADC digital high pass filter, input gain control circuits, and feadphone amplifier. Stereo

24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported. The WM8731 Codec is programmable, it is controlled via a 2 or 3 wire serial interface, the interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities, which can be programmably configured via i2c bus.

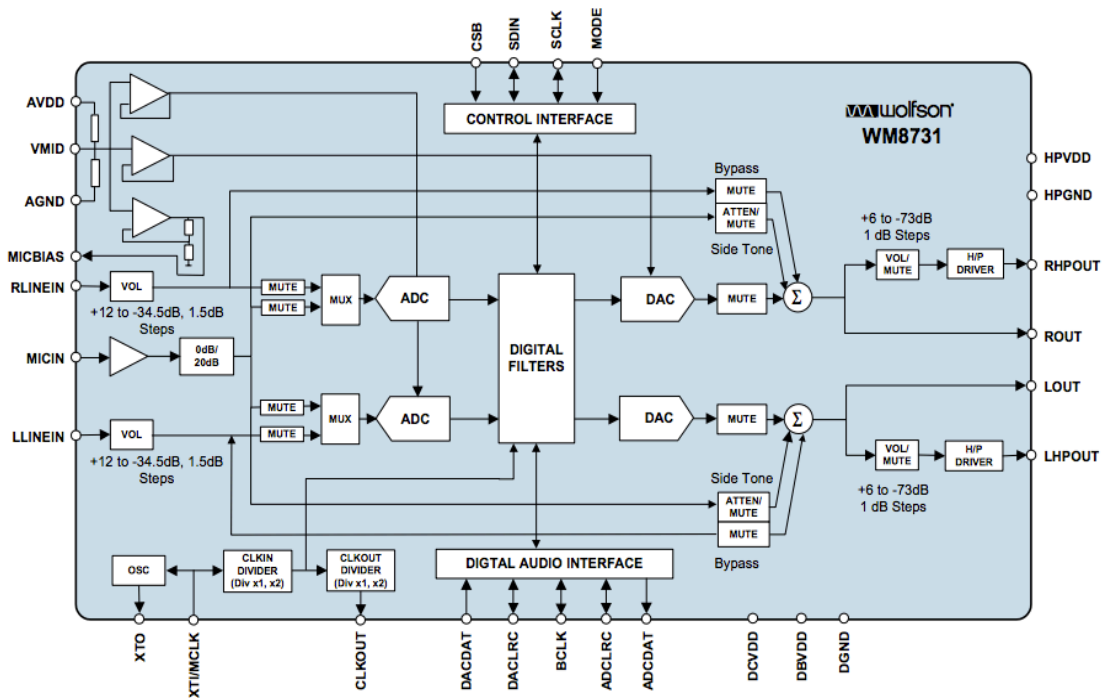


Figure 3 Block diagram of WM8731

Given above is the block diagram of the WM8731 chip. Among all the in/output ports, what we interact the most is the control interface, ADCLRC, ADCDAT, BCLK, MICIN, LOUT. WM8731 has 11 configuration registers, each one contains 9 bits of data and is defined by 7 bits of address. During a write operation, the address and data bits are grouped together to form a 16-bit word and transmitted serially via the I2C bus control to the Codec control interface to initialize the chip. The ADCDAT is the raw digital data coming out of the ADC convertor. ADCLRC is an alignment clock that controls whether left or right channel data is present on the ADCDAT lines. ADCDAT and ADCLRC are synchronous with BCLK signal with

each data bit transition signified by a BCLK high to low transition. BCLK maybe input or output based on whether the Codec is working under master or slave mode. In our case, the chip is working under slave mode.

For the WM8731 clocking schemes, there is only one central source a referenece clock to all the audio data processing progress. The chip is capable of either generating a clock itself with its own on-chip crystal oscillator (18.432MHz), or receiving a clock from an external source. In our design, the Codec will take in an external clock of 25MHz for ADC and DAC process.

I2C Bus Protocol

The WM8731 device can be configured via the control interface, which support 2 or 3 wire serial bus protocol. In our case we applied 2 wire I2Cbus protocol.

I2C stands for Inter-Integrated circuit, it is a low-speed serial bus for efficient communication between device (on-board). Its standard mode support a data rate up to 100K bits per second. I2C bus consists of two bidirectional lines, sda (serial data) and scl (serial clock). These two lines are connected to the sdin and sclk pins of WM8731. During the operation, one device on the bus functions as the master and other devices function as slaves. The master generates the clock on the scl and also initiates and terminates the data transfer. The master and designated slave place data on or retrieve data from sda signal.

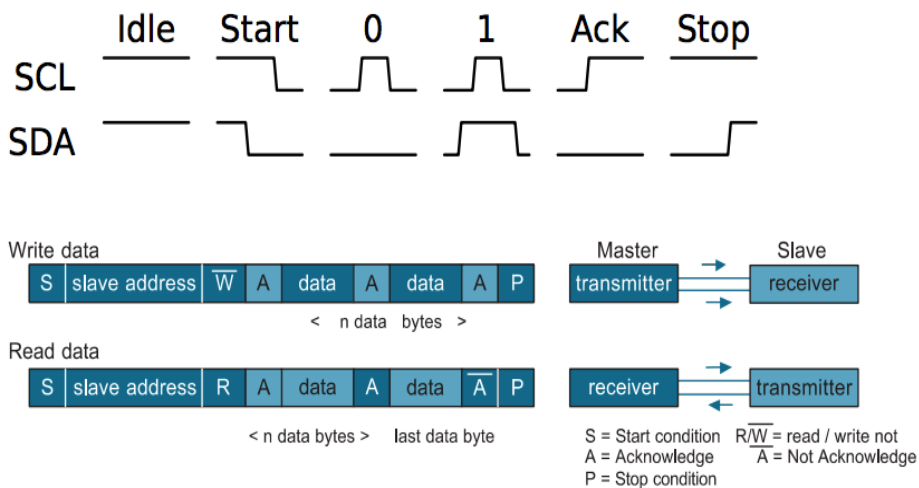


Figure 4 I2C bus Transaction

2.1.1.1 Input

To realize voice control, the whole task is about performing an analog to digital conversion (ADC). The sound that captured by the microphone is analog signals, yet we can only utilize digital signals to perform further computation. Luckily, the WM8731 chip can do the audio ADC for us.

As we have learned above, the WM8731 Codec provided on the DE2 board is programmable, the most important configuration choice we have to make is the sampling rate (8kHz-96kHz) and the analysis (number of bits: 16-32bits). Here we encounter a trade-off between the resource consumption (time, power) and the output quality. Obviously, if more bits are used, the digital data we get from the ADC will be more detailed and contains more information about the original Analog signal, but it will be much slower to compute. It is the same story when comes to higher sampling rate. Our goal here is to try to apply the minimum sampling rate and analysis to achieve the desired conversion quality. Since the ADC input in this application is human voice, which is band-limited to less than 4kHz, so a sampling rate of 8kHz is large enough to handle it. Similarly, 16-bit sampling scheme can offer satisfactory performance as well.

There is one other thing to deal with in audio input. The digital data outputted from the ADC (ADC_DAT) is just a single-bit bit stream, we have to provide a de-serializer to convert this simple 16-bits samples coming out of the Audio Digital Interface into a 16-bit form, which is .WAV form in this case (the sound byte format of .WAV are shown in figure 5). To perform the de-serialization, within a period of the ADC-sampling clock, the de-serializer must be able to convert a 16-bits sample into a single 16-bits word. This requires the de-serializer to run 16 times faster than the sampling clock. Now a new problem presents itself. In our case, the chip runs under the external generated reference clock which is 25MHz, way faster than the target sampling clock and the de-serializer clock. Thus we have to split the clock in a module to get the clocks we want. All this work is carried out in the `de2_wm8731_audio_in` module. We learn about this module from the 2008 MindTones group. Within this component, we set up an array `shift_in : std_logic_vector (15 downto 0)` to store

every 16 raw digital bits in one word. Two dividers are used to split the clock: $lrc_div2 = X"61A"$ slow down the clock to 8kHz (set_lrc) and $bclk_divider2 = X"62"$ is applied to acquire clock running at $8kHz * 16 = 128kHz$ (set_bclk). Running at 8kHz, the byte array will be filled up on every rising edge, then it will be delivered to the audio controller by the signal data_out, after that the controller will put this data on the bus.

Particularly, the sound byte is placed bit by bit into one address of the register, so that when the software read the data from the register, it will get an integer that ranging from 0 to 65,535. Here the two's complement system are applied, the most significant bit of the sound byte is the sign bit. If it is 0, then the integer ranges from 0 to 32,767 represents increasing magnitude. Otherwise, if the 15th bit is 1, the integer ranges from 32,768 to 65,535 in decreasing order of magnitude. In other word, the two opposite ends 0 or 65,535 of the integer range represent minimum magnitude, and the middle section around 32,767 stands for the strongest input.

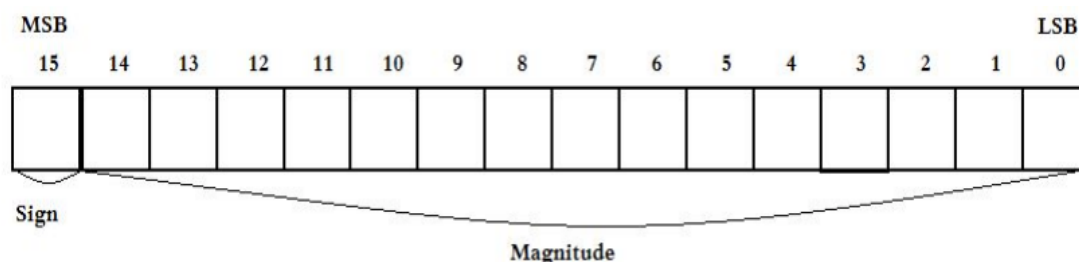


Figure 5 the .WAV sound byte format

2.1.1.2 Output

In output part, we provide background music, as well as sound effect. Sound effect data are stored in ROM, and the background music data are provided by software, which is stored in DRAM in our design.

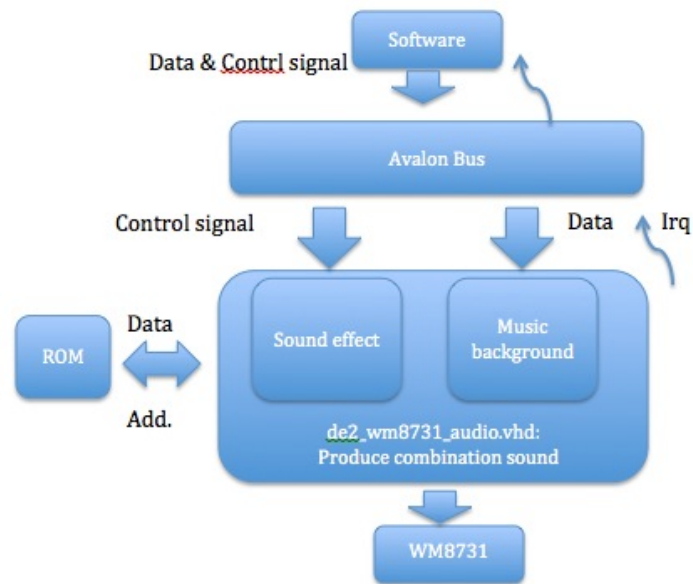


Figure 6 Audio out part architecture

The main audio out program is `de2_wm8731_audio.vhd`, which is built directly in SOPC. The first job of this part is to combine the sound effect and background music together. We put them together by using two sources in different channels. The second job is to get background music, and the third is to get sound effect, as the following two parts show.

For the background music, DRAM is large enough to store our music background data, and each time we provide 31 16-bit data from software through Avalon bus to `audio_out`, by using the offset address 1 to 31. Then the Music background part will output these data one by one, and after sending out all the data, it gives back an Irq signal through Avalon bus to software to request new data.

For the sound effect, every time we provide the address to ROM and get back the data to audio. In ROM, we store 3 sound effects' address serially. This means address from 0 to 6315, 6316 to 10651, 10651 to 16185, stands for 3 different sound effects. Software only needs to provide control signal and tell the hardware when to output and which sound effect to choose, so it just needs one address to provide all sound effects control signals. For each sound effect, software provides the following commands: ($i = 1 \sim 3$)

`IOWR_16DIRECT (AUDIO_BASE, 0, i)`: Set addresses to i sound effect

`IOWR_16DIRECT (AUDIO_BASE, 0, i+1)`: Start to increase the address to output the i sound effect until the i sound effect end address.

Besides, because the restriction of ROM memory, we use 6000Hz as audio frequency. We also get the same sample rates data from .wav file. And to avoid conflicting using of WM8731 ports, de2_wm8731_audio.vhd only has two ports : DACLRC, DACDAT.

2.1.2 VGA Display

Video Display is the most basic part of a video game. Generally the design contains the following aspects.

To store the color data effectively, we use color map to merge 3 colors matrix into one color index matrix. The color map we choose have 216 colors, which is the least number we found that can clearly display the image. The pattern matrix stores 2 hexadecimal numbers for each pixel. When implementing, we first find the color map index in the pattern of the objects. Then using the index we pull the RGB data from the color map matrix. An instance of the color map data is a 24 bits std_logic so that we can get all three RGB color value in just one step. To make the game more alive, we have stored multiple images for one object. In this way, we in some sense achieve animation while game is running.

Generally, we have 4 layers in our VGA display. The basic idea of the layer architecture is that using one process to handle all the elements will cause slow compilation. Moreover, by implementing this way, we easily achieve overlapping relationship, which is due to the different priority of the layers. In our project, the first and uppermost layer contains boss, hitting effect and ammo amount. The next layer includes player, bullet and lives. Enemies and ammo box form the third layer, while the last layer has several background image, game menu and score. For every element, we have two processes one for horizontal, the other for vertical. The processes can use the VGA scanning position, element coordinates and the length and height of the pattern to determine whether or not the image should be displayed.

We have 3 sprites for displaying lives; 5 sprites for displaying armor; 2 sprites for displaying player; 3 sprites for boss Edward, 1 sprite for bullet; 3 sprites for enemies; 1 sprite for firework; 1 sprite for armor box. There shall be one player sprite, one boss sprite and all other

spirates in the screen at the same time.

There are two kinds of communications happens in VGA Controller. The first one is between VGA controller and CPU. There is a buffer in VGA controller that software can write and read. A special process handles the I/O of the buffer. This implementation spares other processes from considering writing and reading data from software. The data in buffer can have several meanings. First, every element's coordinates are controlled by software. Besides, some event flags are given by the software.

The other communication is between VGA controller and SRAM. The data we need from SRAM are background image, game menu image and score images. According to many control signals, VGA controller calculates the address SRAM need and send it to SRAM. SRAM will return the color map index back to VGA controller and then VGA controller can use that information to display the desired image.

We also contains LED display part in our project. It decodes the score values from software and then display the score.

2.1.3 Memory Allocation

To store all the data required in our project, we have implemented several memory components like 32K ROM, 512K SRAM, and 8M SDRAM. That is we used all possible memory devices in our DE2 board.

2.1.3.1 ROM

ROM is basically in charge of sound effects including hitting, laughing and collision. ROM is built using the MegaWizard Manager provided by Quartus II. We created our own .mif file to describe the content of the ROM. We choose to use it to store these date because ROM is fast but small. It is perfect for sound information.

2.1.3.2 SRAM

SRAM takes care of background image, start menu image, game over image and score image. To build a SRAM, we create a separate project

to first write in the data. And then in our main program, we can read the desired data from SRAM without further changing. SRAM is bigger enough to hold the image data we need. Besides, choosing SRAM spare us from frequency problem.

2.1.3.3 SDRAM

CPU uses SDRAM as memory devices. Moreover, BGM is stored in it as well. First, we built SDRAM in SOPC using the controller it provided. Then MegaWizard helps us create a PLL to accordance the clock. At last, we change the CPU memory device to SDRAM. SDRAM is the only left choice we have for CPU memory.

2.2. Software

In our project, software is mainly in charge of audio input categorization, collision detection and game logic. Based on robust hardware design and implementation, the software part is not so hard to realize.

For this project, we use the basic model of Nios processor. This model is fast enough for our design. And to make the game runs properly in time, we create our own clock simulating system in software to control all the events concerning time.

The most unique feature of our game is the audio controller. The hardware provides basic data concerning the audio input. To make the game interesting, we need to further categorize the audio input into 3 kinds. The first one is silence. This is achieved trivially by setting a threshold of audio input value to differentiate sound and silence. The second one is long sound segment, which means the player want the avatar going up. And the last one is a short sound segment, which indicate the avatar should fire. For the last two kinds, we design a special algorithm to discriminate them. Software pull data from Avalon bus every clock time and maintain a variable "flag". This variable "flag" increment whenever it consider the player is making sound. No matter how large or how small is the value of "flag", the avatar will rise up due to audio input. However, if the value of "flag" is between 5 and 9, we assume the player want to shot bullet and thus call create bullet function. Otherwise, if the value of "flag" is greater than 9, we consider the player just want to move and thus do

not call the bullet function. (For the case the value of “flag” is smaller than 5, we think the player is not controlling properly.) Besides, to make the control experience more smoothly, we make the rising up speed according to the intensity of sound. In this manner, we achieve the control of the avatar both movement and shot procedure.

Collision detection is an old idea existing from the beginning of video game. We separate all the stuff in our game into two groups. The first group contains the player and the bullet, while the enemies, ammo box and boss form the other group. In our project, we need to decide if there are collisions between all the combinations of the two groups. Since the objects are not all in regular shape, we create a square core for every object. Only when the core collides with others, we consider a collision happens.

At last, to make the game more interesting, the game logic is pretty complicated. First of all, the game menu needs a stimulus to start the game. We need the player to shout to start the game. Second, the enemies and ammo box are created in a random fashion. The enemies travel horizontally trying to kill the player. Both the enemies and ammo box can be hit by bullet or collided with the player. Collision with enemies will cost the player a life, while with ammo box will provide the player more bullet ammo. Boss initially stays in the rightmost down side of the screen. It will turn from calm to angry and then start moving toward the player. Boss is an advanced enemy that it can move both horizontally and vertically. We use software to instruct hardware to change image for same object so that we can get a sense of animation. In order to prevent multiple collisions in a short period, we implement a “super mode” that keeps the player immortal. Third, the lives and ammos are displayed in the blackboard in the usual manner. And the scores are calculated in a way that counts the time the player alive and the hit it made. Also, the software takes care of informing the hardware to put audio put both background music and sound effects.

Work Division

We have a team of five. As the same order of the previous design flow, the work division is given in the following list.

Name	UNI	Work
Xiaolong Jiang	Xj2137	Audio Input
Junlin Lu	Jl3925	Audio Output
Hongsen Yu	Yh2340	VGA display
Nan Li	Nl2411	Memory allocation
Ji Pei	Jp3242	Software

Challenges & Lesson Learned

1. Hardware

Audio in

I think the trick part to work with WM8371 is concentrated on the control interface. In our case, the `de2_i2c_av_config.v` file contains the configuration data for the WM8731 configuration registers. We start to work on the audio input with the original `de2_12c_av_config.v` file provided in lab3, however there isn't any digital data coming out. We try to change a new microphone, plug it in the LINEIN instead of the MICIN, it still won't work any way. We finally figured out it might be that we fail to initialize the Codec in the right configuration setup. Then we search for resources to this end and find out how the configuration registers initialize the Codec.

In figure 5, it shows what each register can control in detail. We mainly change the data in R2, R3, R4 from the original file. It turns out it is because in the original way, the MUTE MIC function is activated, also, the INSEL field is setup to choose LINEIN as the ADC INPUT source, so there won't be any input sound from the MIC no matter what.

The LHPVOL and RHPVOL field in R2 and R3 are the volume control of the left and right sound track of the headphone. The gain is logarithmically adjustable from +6dB to -73dB in -1dB steps. The LZCEN field is for left zero crossing detect enable, it indicates whether to enable the zero-crossing detection circuit, which can reduce certain click noise. LRHPBOTH field is for left headphone controlling both channels. When it is asserted, the configuration in left channel will be automatically loaded to the right channel.

For R4, the INSEL is the input select, line input is selected if it is 1 and if it's 0, mic input is selected. The functions of other fields can be implied from its name, basically 1 is on and 0 is off. After we decided what configuration we need and fill up the register in binary field, we should translate it into hexadecimal field, because in the i2c bus the data is written in hex.

register	address	data								
	B15 - B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R0	000000	LRIN BOTH	LIN MUTE	0	0	LINVOL				
R1	000001	RRIN BOTH	RIN MUTE	0	0	RINVOL				
R2	000010	LRHP BOTH	LZCEN	LHPVOL						
R3	000011	RRHP BOTH	RZCEN	RHPVOL						
R4	000100	0	SIDEATT	SIDE TONE	DAC SEL	BYPASS	INSEL	MUTE MIC	MIC BOOST	
R5	000101	0	0	0	0	HPOR	DAC MU	DEEMPH	ADC HPD	
R6	000110	0	PPW OFF	CLK OUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LININPD
R7	000111	0	BCLK INV	MS	LR SWAP	LRP	IWL	FORMAT		
R8	001000	0	CLKO DIV2	CLKI DIV2	SR				BOSR	USB/ NORM
R9	001001	0	0	0	0	0	0	0	ACTIVE	
R15	001111	RESET								

Figure 7 WM8731 register map

The LHPVOL and RHPVOL field in R2 and R3 are the volume control of the left and right sound track of the headphone. For R4, the INSEL is the input select, line input is selected if it is 1 and if it's 0, mic input is selected. The functions of other fields can be implied from its name, basically 1 is on and 0 is off. After we decided what configuration we need and fill up the register in binary field, we should translate it into hexadecimal field, because in the i2c bus the data is written in hex.

Audio out

1. Figure out the clock divider meaning in sample program, and calculate the proper clock frequency.
2. Because of the uncertainty of memory using, I have to figure out

how to read and output the sound in each memory.

3. Address counter for sound effect is a little bit confusion, because I need to output it only once after getting one command, and also set the initial address and end address for each sound effect.

4. Do not code the same file in two or more programs at the same time, or you may miss some modification.

5. When doing large scale replacing of code, do it in gedit, rather than in Quartus or Nios2. The latter is much slower, and may leads to program crash.

6. In software, to store many data in array, use "const" before "int", or it cannot access the DRAM, and produce error.

VGA Display

In the part of VGA display, the most difficult problem we are facing is to reduce compilation time. Because we are storing and processing a lot of data, an efficient algorithm is desperately needed. The first problem we realize is that in color map matrix we need to concatenate RGB information into one element instead of 3 different elements. Besides, we use different processes to achieve pipeline to make the whole program run faster.

Memory Allocation

The most difficult part we think is to invoke data from SRAM to VGA. It is hard to figure out how to translate the pixels in VGA monitor to SRAM address. At last, we found that there is a linear relationship between them. An easily overlooked but important thing we found is that when calculating the address from the pixels we need to deduct one more point.

2. Software

The most challenging part of software is to figure out an efficient algorithm for determining audio input. The algorithm needs to be real-time and precise. The algorithm we came out is a straightforward way. We have tried many different ways to implement that like using hardware to determine or keeping an array

to store the sound information. However, we found this one can provide the most playable result we want.

Future Idea

In the future, we think there mainly are two ways to improve Ah-Ah-Piu. First of all, we can make the game more interesting by adding up new cool features. For instance, now the player can only destroy the enemies by shooting a bullet, we should design new weapons maybe like grenade or missiles that can cause larger damage not only along a straight line, but also within an area. Moreover, We can implements a super weapon like a nuclear bomb, which can be triggered by a super loud shout and will clear out all the enemies on the whole screen. Other than new manners to attack, we may as well as try to add up lives supplies in the same logic like the ammo supply we currently have.

By now the sound control mechanisms we have are working with magnitude. We think implementing some frequency analysis algorithm on the hardware to support frequency control mode is a good game experience for players. Besides just sound control, keyboard control or game controller may also be very interesting to play with as well.

Source Code

Lab3_vga.vhd, our top-level entity for the main project

```
-- DE2 top-level module that includes the simple VGA raster generator
--
-- Stephen A. Edwards, Columbia University, sedwards@cs.columbia.edu
--
-- From an original by Terasic Technology, Inc.
-- (DE2_TOP.v, part of the DE2 system board CD supplied by Altera)
--
```

```
library ieee;
```

```
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity lab3_vga is

  port (
    -- Clocks

    CLOCK_27,                -- 27 MHz
    CLOCK_50,                -- 50 MHz
    EXT_CLOCK : in std_logic; -- External Clock

    -- Buttons and switches

    KEY : in std_logic_vector(3 downto 0); -- Push buttons
    SW  : in std_logic_vector(17 downto 0); -- DPDT switches

    -- LED displays

    HEX0, HEX1, HEX2, HEX3, HEX4, HEX5, HEX6, HEX7 -- 7-segment displays
      : out std_logic_vector(6 downto 0);
    LEDG : out std_logic_vector(8 downto 0); -- Green LEDs
    LEDR : out std_logic_vector(17 downto 0); -- Red LEDs

    -- RS-232 interface

    UART_TXD : out std_logic; -- UART transmitter
    UART_RXD : in std_logic;  -- UART receiver

    -- IRDA interface

    -- IRDA_TXD : out std_logic; -- IRDA Transmitter
    IRDA_RXD : in std_logic;    -- IRDA Receiver

    -- SDRAM

    DRAM_DQ : inout std_logic_vector(15 downto 0); -- Data Bus
    DRAM_ADDR : out std_logic_vector(11 downto 0); -- Address Bus
    DRAM_LDQM,                -- Low-byte Data Mask
    DRAM_UDQM,                -- High-byte Data Mask
    DRAM_WE_N,                -- Write Enable
    DRAM_CAS_N,               -- Column Address Strobe
    DRAM_RAS_N,               -- Row Address Strobe
    DRAM_CS_N,                -- Chip Select
```

```
DRAM_BA_0,                -- Bank Address 0
DRAM_BA_1,                -- Bank Address 0
DRAM_CLK,                 -- Clock
DRAM_CKE : out std_logic; -- Clock Enable

-- FLASH

FL_DQ : inout std_logic_vector(7 downto 0); -- Data bus
FL_ADDR : out std_logic_vector(21 downto 0); -- Address bus
FL_WE_N,                  -- Write Enable
FL_RST_N,                 -- Reset
FL_OE_N,                  -- Output Enable
FL_CE_N : out std_logic;  -- Chip Enable

-- SRAM

SRAM_DQ : inout std_logic_vector(15 downto 0); -- Data bus 16 Bits
SRAM_ADDR : out std_logic_vector(17 downto 0); -- Address bus 18 Bits
SRAM_UB_N,                -- High-byte Data Mask
SRAM_LB_N,                -- Low-byte Data Mask
SRAM_WE_N,                -- Write Enable
SRAM_CE_N,                -- Chip Enable
SRAM_OE_N : out std_logic; -- Output Enable

-- USB controller

OTG_DATA : inout std_logic_vector(15 downto 0); -- Data bus
OTG_ADDR : out std_logic_vector(1 downto 0);    -- Address
OTG_CS_N,                -- Chip Select
OTG_RD_N,                -- Write
OTG_WR_N,                -- Read
OTG_RST_N,               -- Reset
OTG_FSPEED,              -- USB Full Speed, 0 = Enable, Z = Disable
OTG_LSPEED : out std_logic; -- USB Low Speed, 0 = Enable, Z = Disable
OTG_INT0,                -- Interrupt 0
OTG_INT1,                -- Interrupt 1
OTG_DREQ0,               -- DMA Request 0
OTG_DREQ1 : in std_logic; -- DMA Request 1
OTG_DACK0_N,             -- DMA Acknowledge 0
OTG_DACK1_N : out std_logic; -- DMA Acknowledge 1

-- 16 X 2 LCD Module

LCD_ON,                  -- Power ON/OFF
```

```
LCD_BLON,                -- Back Light ON/OFF
LCD_RW,                  -- Read/Write Select, 0 = Write, 1 = Read
LCD_EN,                  -- Enable
LCD_RS : out std_logic;  -- Command/Data Select, 0 = Command, 1 = Data
LCD_DATA : inout std_logic_vector(7 downto 0); -- Data bus 8 bits

-- SD card interface

SD_DAT,                  -- SD Card Data
SD_DAT3,                 -- SD Card Data 3
SD_CMD : inout std_logic; -- SD Card Command Signal
SD_CLK : out std_logic;  -- SD Card Clock

-- USB JTAG link

TDI,                     -- CPLD -> FPGA (data in)
TCK,                     -- CPLD -> FPGA (clk)
TCS : in std_logic;      -- CPLD -> FPGA (CS)
TDO : out std_logic;     -- FPGA -> CPLD (data out)

-- I2C bus

I2C_SDAT : inout std_logic; -- I2C Data
I2C_SCLK : out std_logic;   -- I2C Clock

-- PS/2 port

PS2_DAT,                 -- Data
PS2_CLK : in std_logic;  -- Clock

-- VGA output

VGA_CLK,                 -- Clock
VGA_HS,                  -- H_SYNC
VGA_VS,                  -- V_SYNC
VGA_BLANK,               -- BLANK
VGA_SYNC : out std_logic; -- SYNC
VGA_R,                   -- Red[9:0]
VGA_G,                   -- Green[9:0]
VGA_B : out std_logic_vector(9 downto 0); -- Blue[9:0]

-- Ethernet Interface

ENET_DATA : inout std_logic_vector(15 downto 0); -- DATA bus 16Bits
```

```

ENET_CMD,          -- Command/Data Select, 0 = Command, 1 = Data
ENET_CS_N,         -- Chip Select
ENET_WR_N,        -- Write
ENET_RD_N,        -- Read
ENET_RST_N,       -- Reset
ENET_CLK : out std_logic; -- Clock 25 MHz
ENET_INT : in std_logic;  -- Interrupt

-- Audio CODEC

AUD_ADCLRCK : inout std_logic; -- ADC LR Clock
AUD_ADCDATA : in std_logic;    -- ADC Data
AUD_DACLCK : inout std_logic;  -- DAC LR Clock
AUD_DACDATA : out std_logic;   -- DAC Data
AUD_BCLK : inout std_logic;    -- Bit-Stream Clock
AUD_XCK : out std_logic;      -- Chip Clock

-- Video Decoder

TD_DATA : in std_logic_vector(7 downto 0); -- Data bus 8 bits
TD_HS,          -- H_SYNC
TD_VS : in std_logic; -- V_SYNC
TD_RESET : out std_logic; -- Reset

-- General-purpose I/O

GPIO_0,          -- GPIO Connection 0
GPIO_1 : inout std_logic_vector(35 downto 0) -- GPIO Connection 1
);

end lab3_vga;

```

architecture datapath of lab3_vga is

```

signal clk25 : std_logic := '0';
signal reset_n : std_logic;
signal BA : STD_LOGIC_VECTOR(1 downto 0);
signal DQM : STD_LOGIC_VECTOR(1 downto 0);
signal pll_c1: STD_LOGIC;

begin

process (CLOCK_50)
begin

```

```

if rising_edge(CLOCK_50) then
    clk25 <= not clk25;
end if;
end process;

```

V1: entity work.nios_system port map (

```

    reset_n => '1',
    clk_0    => clk25,

    SRAM_ADDR_from_the_sram    => SRAM_ADDR,
    SRAM_CE_N_from_the_sram    => SRAM_CE_N,
    SRAM_DQ_to_and_from_the_sram => SRAM_DQ,
    SRAM_LB_N_from_the_sram    => SRAM_LB_N,
    SRAM_OE_N_from_the_sram    => SRAM_OE_N,
    SRAM_UB_N_from_the_sram    => SRAM_UB_N,
    SRAM_WE_N_from_the_sram    => SRAM_WE_N,

    zs_addr_from_the_sdram     => DRAM_ADDR,
    zs_ba_from_the_sdram       => BA,
    zs_cas_n_from_the_sdram    => DRAM_CAS_N,
    zs_cke_from_the_sdram      => DRAM_CKE,
    zs_cs_n_from_the_sdram     => DRAM_CS_N,
    zs_dq_to_and_from_the_sdram => DRAM_DQ,
    zs_dqm_from_the_sdram      => DQM,
    zs_ras_n_from_the_sdram    => DRAM_RAS_N,
    zs_we_n_from_the_sdram     => DRAM_WE_N

);

```

neg_3ns: entity work.sdram_pll port map(

```

    inclk0 => CLOCK_50,
    c0     => DRAM_CLK,
    c1     => pll_c1);

    HEX7    <= "0001001"; -- Leftmost
    HEX6    <= "0000110";
    HEX5    <= "1000111";
    HEX4    <= "1000111";
    HEX3    <= "1000000";
    HEX2    <= (others => '1');
    HEX1    <= (others => '1');
    HEX0    <= (others => '1');          -- Rightmost
    LEDG    <= (others => '1');
    LEDR    <= (others => '1');

```



```
LCD_ON    <= '1';
LCD_BLON <= '1';
LCD_RW <= '1';
LCD_EN <= '0';
LCD_RS <= '0';

SD_DAT3 <= '1';
SD_CMD <= '1';
SD_CLK <= '1';
UART_TXD <= '0';
DRAM_LDQM <= DQM(0);
DRAM_UDQM <= DQM(1);
DRAM_BA_0 <= BA(0);
DRAM_BA_1 <= BA(1);

FL_ADDR <= (others => '0');
FL_WE_N <= '1';
FL_RST_N <= '0';
FL_OE_N <= '1';
FL_CE_N <= '1';
OTG_ADDR <= (others => '0');
OTG_CS_N <= '1';
OTG_RD_N <= '1';
OTG_RD_N <= '1';
OTG_WR_N <= '1';
OTG_RST_N <= '1';
OTG_FSPPEED <= '1';
OTG_LSPPEED <= '1';
OTG_DACK0_N <= '1';
OTG_DACK1_N <= '1';

TDO <= '0';

ENET_CMD <= '0';
ENET_CS_N <= '1';
ENET_WR_N <= '1';
ENET_RD_N <= '1';
ENET_RST_N <= '1';
ENET_CLK <= '0';

TD_RESET <= '0';

I2C_SCLK <= '1';
```

```

AUD_DACDAT <= '1';
AUD_XCK <= '1';

FL_DQ      <= (others => 'Z');

OTG_DATA   <= (others => 'Z');
LCD_DATA   <= (others => 'Z');
SD_DAT     <= 'Z';
I2C_SDAT   <= 'Z';
ENET_DATA  <= (others => 'Z');
AUD_ADCLRCK <= 'Z';
AUD_DACLCK <= 'Z';
AUD_BCLK   <= 'Z';
GPIO_0     <= (others => 'Z');

end datapath;

de2_wm8731_audio_in.vhd, Our module used to de-serialize the bit-stream
outputted from the ADC into 16-bits .WAV format sound byte
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- This module do the de-serialize which transform the ADCDAT bit-stream to 16-bits sound byte
-- de2_wm8731_audio_in : generate clock and get the samples from device

entity de2_wm8731_audio_in is
port (
    clk : in std_logic;          -- external generated reference clock 25MHz
    reset_n : in std_logic;
    data_out : out std_logic_vector(15 downto 0);
    audio_req : out std_logic;

    -- Audio interface signals
    AUD_ADCLRCK : out std_logic;  -- Audio CODEC ADC LR Clock
    AUD_ADCDAT : in std_logic;    -- Audio CODEC ADC Data
    AUD_BCLK : inout std_logic;   -- Audio CODEC Bit-Stream Clock
);
end de2_wm8731_audio_in;

```

architecture Behavioral of de2_wm8731_audio_in is

```

signal lrck : std_logic;
signal bclk : std_logic;
signal xck : std_logic;

signal lrck_divider : std_logic_vector (7 downto 0);
signal bclk_divider : std_logic_vector (3 downto 0);

signal set_bclk : std_logic;
signal set_lrck : std_logic;
signal lrck_lat : std_logic;
signal clr_bclk : std_logic;
signal datain : std_logic;

signal shift_in : std_logic_vector ( 15 downto 0);
signal shift_counter : integer := 15;

-- Second clock divider

signal lrck_div2 : std_logic_vector (11 downto 0);
--signal set_lrck2 : std_logic;
signal bclk_divider2: std_logic_vector (7 downto 0);

begin
  -- LRCK divider
  -- Audio system clock / Sample rate 8KHz
  -- Divider is 25MHz/1562 = 8KHz
  -- Left justify mode set by I2C controller

  process(clk, reset_n) -- loops Another divider to slow down the LRclk
  begin
    if ( reset_n = '0' ) then
      lrck_div2 <= (others => '0');
    elsif ( clk'event and clk='1' ) then
      if ( lrck_div2 = X"61A" ) then      -- 8FF = 900 - 1
        lrck_div2 <= X"000";
      else
        lrck_div2 <= lrck_div2 + '1';
      end if;
    end if;
  end process;

  process(clk, reset_n) -- loops second bclk_divider -- we only need one of the 2

```

```

begin
  if ( reset_n = '0' ) then
    bclk_divider2 <= (others => '0');
  elsif ( clk'event and clk='1' ) then
    if ( bclk_divider2 = X"62" or set_lrck = '1')  then    -- 8F = 90-1
      bclk_divider2 <= X"00";
    else
      bclk_divider2 <= bclk_divider2 + '1';
    end if;
  end if;
end process;

```

```

process ( lrck_div2 )
begin
  if ( lrck_div2 = X"61A") then
    set_lrck <= '1';
  else
    set_lrck <= '0';
  end if;
end process;

```

-- Here we just have to change set_lrck to set_lrck2 to change the Sampling rate to 8kHz

```

process ( clk, reset_n)
begin
  if ( reset_n = '0') then
    lrck <= '0';
  elsif ( clk 'event and clk = '1') then
    if ( set_lrck = '1') then
      lrck <= not lrck;
    end if;
  end if;
end process;

```

```

-- BCLK divider
process ( bclk_divider2 )
begin
  if ( bclk_divider2 = X"31") then
    set_bclk <= '1';
  else
    set_bclk <= '0';
  end if;

  if ( bclk_divider2 = X"62") then -- xB

```

```
        clr_bclk <= '1';
    else
        clr_bclk <= '0';
    end if;
end process;

process ( clk, reset_n)
begin
    if ( reset_n = '0') then
        bclk <= '0';
    elsif ( clk 'event and clk = '1') then
        if ( set_lrck = '1' or clr_bclk = '1') then
            bclk <= '0';
        elsif ( set_bclk = '1') then
            bclk <= '1';
        end if;
    end if;
end process;

process (clk)
begin
    if ( clk 'event and clk = '1') then
        if (set_bclk = '1') then
            shift_in(shift_counter) <= AUD_ADCDAT;
            if (shift_counter = 0) then
                shift_counter <= 15;
            else
                shift_counter <= shift_counter - 1;
            end if;
        end if;
    end if;
end process;

process(clk)
begin
    if ( clk'event and clk='1' ) then -- why??
        lrck_lat <= lrck;
    end if;
end process;

process ( clk, reset_n)
begin
    if ( clk 'event and clk = '1') then
```

```

        if ( set_lrck = '1') then
            data_out <= shift_in;
            audio_req <= '1';
        else
            audio_req <='0';
        end if;
    end if;
end process;

-- Audio outputs

AUD_BCLK    <= bclk;
AUD_ADCLRCK <= lrck;

end architecture;
```

de2_wm8731_audio.vhd, used for the audio output

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity de2_wm8731_audio is
port (
    clk : in std_logic;          -- Audio CODEC Chip Clock AUD_XCK (18.43 MHz)
    reset_n : in std_logic;
    request : out std_logic;
    rom_read : in std_logic_vector(15 downto 0);
    rom_addr: out std_logic_vector (13 downto 0);

    -- data : in std_logic_vector(15 downto 0);
    -- VGA_LED : out std_logic_vector (26 downto 0);
    read : in std_logic;
    write : in std_logic;
    chipselect : in std_logic;
    address : in std_logic_vector(5 downto 0);
    readdata : out std_logic_vector(15 downto 0);
    writedata : in std_logic_vector(15 downto 0);

    -- Audio interface signals
    -- AUD_ADCLRCK : out std_logic; -- Audio CODEC ADC LR Clock
    --AUD_ADCDAT : in std_logic; -- Audio CODEC ADC Data
```

```

    AUD_DACLCK  : out  std_logic;  --  Audio CODEC DAC LR Clock
    AUD_DACDAT  : out  std_logic  --  Audio CODEC DAC Data
--   AUD_BCLK   : inout std_logic  --  Audio CODEC Bit-Stream Clock
  );
end  de2_wm8731_audio;

```

architecture rtl of de2_wm8731_audio is

```

    signal lrck : std_logic;
    signal bclk : std_logic;
--   signal xck  : std_logic;

    signal lrck_divider : unsigned (15 downto 0);
    signal bclk_divider : unsigned (11 downto 0);
    signal sin_out      : unsigned(15 downto 0);
    signal set_bclk : std_logic;
    signal set_lrck : std_logic;
    signal clr_bclk : std_logic;
    signal lrck_lat : std_logic;
    signal endOfTone : unsigned (13 downto 0);
    signal shift_out : std_logic_vector(15 downto 0);

    signal mark : std_logic;

    signal sin_counter : unsigned (13 downto 0);
    signal bac_counter : unsigned (4 downto 0);
    signal shift_before : std_logic_vector(7 downto 0);

    type ram_type is array(31 downto 0) of
        std_logic_vector(15 downto 0);
    signal RAM : ram_type:= (
        others=>"0000000000000000"
    );
    signal ram_address: unsigned(4 downto 0);

    signal switch : std_logic ;
    signal  sin_out0,sin_out1,sin_out2 : unsigned(15 downto 0);
    signal merged: unsigned (15 downto 0)

```

begin

```

    ram_address <= unsigned(address(4 downto 0));

```

```

process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      readdata <= (others => '0');
    else
      if chipselect = '1' then
        if read = '1' then
          readdata <= RAM( to_integer( ram_address));
        elsif write = '1' then
          RAM(to_integer (ram_address)) <= writedata;
        end if;
      end if;
    end if;
  end if;
end process;

process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      lrck_divider <= (others => '0');
    elsif lrck_divider = X"1047" then -- "C0" minus 1 822
      lrck_divider <= X"0000";
    else
      lrck_divider <= lrck_divider + 1;
    end if;
  end if;
end process;

process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      bclk_divider <= (others => '0');
    elsif bclk_divider = X"104" or set_lrck = '1' then ---81
      bclk_divider <= X"000";
    else
      bclk_divider <= bclk_divider + 1;
    end if;
  end if;
end process;

```



```

set_lrck <= '1' when lrck_divider = X"1047" else '0'; --822

process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      lrck <= '0';
    elsif set_lrck = '1' then
      lrck <= not lrck;
    end if;
  end if;
end process;

-- BCLK divider
set_bclk <= '1' when bclk_divider(11 downto 0) = X"082" else '0';--40
clr_bclk <= '1' when bclk_divider(11 downto 0) = X"104" else '0';--81

process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      bclk <= '0';
    elsif set_lrck = '1' or clr_bclk = '1' then
      bclk <= '0';
    elsif set_bclk = '1' then
      bclk <= '1';
    end if;
  end if;
end process;

-- Audio data shift output
process (clk)
begin
  if rising_edge(clk) then
    if switch = '0' then
      merged <= unsigned(RAM(to_integer(bac_counter)));
      -----8 bit-----
-----8 bit-----
    else
      --merged <= sin_out;
merged <= unsigned(rom_read);
    end if;

    if reset_n = '0' then

```

```
    shift_out <= (others => '0');
elseif set_lrck = '1' then

    shift_out <= std_logic_vector (merged);

elseif clr_bclk = '1' then
    shift_out <= shift_out (14 downto 0) & '0';
end if;
end if;
end process;

process(clk)
begin
if rising_edge(clk) then
if reset_n = '0' or RAM(0) = "0000000000000000"then
-- if reset_n = '0' then
sin_counter <= (others => '0');
--dead--
elseif RAM(0) = "0000000000000001"then
sin_counter <= (others => '0');
--hitting--
elseif RAM(0) = "0000000000000011"then
sin_counter <= "01100010101010";
--laugh--
elseif RAM(0) = "0000000000000101"then
sin_counter <= "10100110011010";
elseif
lrck_lat = '1' and lrck = '0' and sin_counter < endOfTone then

sin_counter <= sin_counter + 1;
switch <= not switch ;

end if;
end if;
end process;

process(clk)
begin
if rising_edge(clk) then
if reset_n = '0' then
```

```
        bac_counter <= "00001";
    elsif lrck_lat = '1' and lrck = '0' then
        if bac_counter = "11111" then

            bac_counter <= "00001";
        else
            bac_counter <= bac_counter + 1;

        end if;
    end if;
end if;
end process;

--reset the request signal
process (clk)
begin
    if rising_edge(clk) then
        if reset_n = '0' then
            request <= '0';
        else
            if bac_counter = "11111" then
                request <= '1';
            elsif write = '1' and chipselect = '1' then
                request <= '0'; -- important to reset the irq
            end if;
        end if;
    end if;
end process;

process(clk)
begin
    if rising_edge(clk) then
        lrck_lat <= lrck;
    end if;
end process;

--ending time and effect sound select
-- sin_out <= sin_out0;
-- endOfTone <= "0100010011011";
endOfTone <= "01100010101010" when RAM(0) = "0000000000000001" or RAM(0) =
"0000000000000010" else
    "10100110011010" when RAM(0) = "0000000000000011" or RAM(0) =
"0000000000000100" else
```

```

        "11111100111000" when RAM(0) = "0000000000000101" or RAM(0) =
"0000000000000110" else
        "11111100111000";

--sin_out <= sin_out0 when RAM(0) = "0000000000000010" else
--      sin_out1 when RAM(0) = "0000000000000001" else
--      sin_out0;

        --output address counter
    process (clk)
    begin
        if rising_edge(clk) then
            if reset_n = '0' then
                rom_addr <= (others => '0');
            else
                rom_addr <= std_logic_vector(sin_counter);
            end if;
        end if;
    end process;
end architecture;

```

de2_vga_raster.vhd, **used for the vga display**

```

-----
--
-- VGA main display part by Hongsen Yu
--
-- Build it as top in SOPC
--
--
-----
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity de2_vga_raster is

    port (
        reset_n : in std_logic;
        clk50    : in std_logic;      -- Should be 25.125 MHz
        sram_read : in std_logic_vector(15 downto 0);

```

```

sram_add  : out std_logic_vector (17 downto 0);
read      : in  std_logic;
write     : in  std_logic;
chipselect : in  std_logic;
address   : in  std_logic_vector(4 downto 0);
readdata  : out std_logic_vector(15 downto 0);
writedata : in  std_logic_vector(15 downto 0);
VGA_CLK,                                     -- Clock
VGA_HS,                                       -- H_SYNC
VGA_VS,                                       -- V_SYNC
VGA_BLANK,                                    -- BLANK
VGA_SYNC : out std_logic;                    -- SYNC
VGA_R,                                        -- Red[9:0]
VGA_G,                                        -- Green[9:0]
VGA_B : out std_logic_vector(9 downto 0) -- Blue[9:0]
);

end de2_vga_raster;

```

architecture rtl of de2_vga_raster is

```

component V_control
  port(
    clk      : in std_logic;
    Vcount   : in unsigned(9 downto 0);
    Pattern_V : in integer;
    locate   : in integer;
    Vcounter : out integer;
    flag_v   : out std_logic;
    reset_n  : in std_logic;
    EndofLine : in std_logic
  );
end component;

```

```

component H_control
  port(
    clk      : in std_logic;
    Hcount   : in unsigned(9 downto 0);
    Pattern_H : in integer;
    locate   : in integer;
    Hcounter : out integer;
    flag_h   : out std_logic
  );
end component;

```

-- Video parameters

```
constant HTOTAL      : integer := 800;
constant HSYNC       : integer := 96;
constant HBACK_PORCH : integer := 48;
constant HACTIVE     : integer := 640;
constant HFRONT_PORCH : integer := 16;
```

```
constant VTOTAL      : integer := 525;
constant VSYNC       : integer := 2;
constant VBACK_PORCH : integer := 33;
constant VACTIVE     : integer := 480;
constant VFRONT_PORCH : integer := 10;
```

```
constant RECTANGLE_HSTART : integer := 100;
constant RECTANGLE_HEND   : integer := 540;
constant RECTANGLE_VSTART : integer := 100;
constant RECTANGLE_VEND   : integer := 380;
constant PATTERN_V : integer :=80;
constant PATTERN_H : integer :=60;
constant PATTERN_V_C : integer :=60;
constant PATTERN_H_C : integer :=60;
constant PATTERN_V_E : integer :=80;
constant PATTERN_H_E : integer :=60;
constant PATTERN_V_B : integer :=25;
constant PATTERN_H_B : integer :=66;
```

-- Signals for the video controller

```
signal clk : std_logic;
signal Hcount : unsigned(9 downto 0); -- Horizontal position (0-800)
signal Vcount : unsigned(9 downto 0); -- Vertical position (0-524)
signal EndOfLine, EndOffield : std_logic;
signal Hcounter : integer :=0 ;
signal Vcounter : integer :=0 ;
signal Hcounter_B : integer :=0 ;
signal Vcounter_B : integer :=0 ;
signal Hcounter_C : integer :=0 ;
signal Vcounter_C : integer :=0 ;
signal Hcounter_E : integer :=0 ;
signal Vcounter_E : integer :=0 ;
signal Hcounter_E1 : integer :=0 ;
signal Vcounter_E1 : integer :=0 ;
signal Hcounter_E2 : integer :=0 ;
```

```
signal Vcounter_E2 : integer :=0 ;
signal Hcounter_E3 : integer :=0 ;
signal Vcounter_E3 : integer :=0 ;
signal Hcounter_BOX : integer :=0 ;
signal Vcounter_BOX : integer :=0 ;
signal Hcounter_BM : integer :=0 ;
signal Vcounter_BM : integer :=0 ;
signal Hcounter_LV1 : integer :=0 ;
signal Vcounter_LV1 : integer :=0 ;
signal Hcounter_LV2 : integer :=0 ;
signal Hcounter_LV3 : integer :=0 ;
signal Vcounter_BU : integer :=0 ;
signal Hcounter_BU1 : integer :=0 ;
signal Hcounter_BU2 : integer :=0 ;
signal Hcounter_BU3 : integer :=0 ;
signal Hcounter_BU4 : integer :=0 ;
signal Hcounter_BU5 : integer :=0 ;
signal cmpindex1 : integer :=0;
signal cmpindex2 : integer :=0;
signal cmpindex3 : integer :=0;
signal cmpindex4 : integer :=0;
signal cmpindex5 : integer :=0;
signal cmpindex6 : integer :=0;
signal cmpindex8 : integer :=0;
signal cmpindexLV1 : integer :=0;
signal cmpindexLV2 : integer :=0;
signal cmpindexLV3 : integer :=0;
signal cmpindexBU1 : integer :=0;
signal cmpindexBU2 : integer :=0;
signal cmpindexBU3 : integer :=0;
signal cmpindexBU4 : integer :=0;
signal cmpindexBU5 : integer :=0;
signal cmpindexBOX : integer :=0;
signal LEVEL_3_R : std_logic_vector(9 downto 0);
signal LEVEL_3_G : std_logic_vector(9 downto 0);
signal LEVEL_3_B : std_logic_vector(9 downto 0);
signal LEVEL_2_R : std_logic_vector(9 downto 0);
signal LEVEL_2_G : std_logic_vector(9 downto 0);
signal LEVEL_2_B : std_logic_vector(9 downto 0);
signal LEVEL_1_R : std_logic_vector(9 downto 0);
signal LEVEL_1_G : std_logic_vector(9 downto 0);
signal LEVEL_1_B : std_logic_vector(9 downto 0);
signal LEVEL_0_R : std_logic_vector(9 downto 0);
signal LEVEL_0_G : std_logic_vector(9 downto 0);
```

```

signal LEVEL_0_B : std_logic_vector(9 downto 0);
signal level_0 : std_logic := '0';
signal level_1 : std_logic := '0';
signal level_2 : std_logic := '0';
signal level_3 : std_logic := '0';
signal hcounter_s : integer := 0;
signal vcounter_s : integer := 0;
signal mark : std_logic ;

```

```

type Array0 is array(0 to 215) of std_logic_vector(23 downto 0);
type Array1 is array( 0 to 4799) of std_logic_vector(7 downto 0);
type Array2 is array( 0 to PATTERN_V_B*PATTERN_H_B-1) of std_logic_vector(7 downto 0);
type Array3 is array( 0 to PATTERN_V_C*PATTERN_H_C-1) of std_logic_vector(7 downto 0);
type Array4 is array( 0 to PATTERN_V_E*PATTERN_H_E-1) of std_logic_vector(7 downto 0);
type Array5 is array( 0 to 899) of std_logic_vector(7 downto 0);
type Array6 is array( 0 to 2999) of std_logic_vector(7 downto 0);
type Array7 is array(0 to 919) of std_logic_vector(7 downto 0);
type Array8 is array(0 to 2759)of std_logic_vector(7 downto 0);

```

```

constant colormap: Array0 :=(
"1111111111111111111111111", "11111111111111111001110", "11111111111111100110
01", "11111111111111101100110", "11111111111111100110011", "111111111111111000
00000",
"1111111111001100111111111", "111111111100110011001100", "1111111111001100100110
01", "111111111100110001100110", "111111111100110000110011", "1111111111001100000
0000",
"1111111111001100111111111", "1111111111001100111001100", "11111111110011001100110
01", "1111111111001100101100110", "1111111111001100100110011", "11111111110011001000
0000",
"1111111101100110111111111", "111111110110011011001100", "1111111101100110100110
01", "111111110110011001100110", "111111110110011000110011", "1111111101100110000
0000",
"1111111100110011111111111", "111111110011001111001100", "1111111100110011100110
01", "111111110011001101100110", "111111110011001100110011", "1111111100110011000
0000",
"1111111100000000111111111", "111111110000000011001100", "1111111100000000100110
01", "111111110000000001100110", "111111110000000000110011", "1111111100000000000
0000",
"1100110011111111111111111", "110011001111111111001100", "11001100111111111100110
01", "1100110011111111101100110", "1100110011111111100110011", "11001100111111111000
0000",
"1100110011001100111111111", "110011001100110011001100", "1100110011001100100110
01", "110011001100110001100110", "110011001100110000110011", "1100110011001100000

```


00000",
"11001100100110011111111111", "110011001001100111001100", "1100110010011001100110
01", "110011001001100101100110", "110011001001100100110011", "1100110010011001000
00000",
"11001100011001101111111111", "110011000110011011001100", "1100110001100110100110
01", "110011000110011001100110", "110011000110011000110011", "1100110001100110000
00000",
"11001100001100111111111111", "110011000011001111001100", "1100110000110011100110
01", "110011000011001101100110", "110011000011001100110011", "1100110000110011000
00000",
"11001100000000001111111111", "110011000000000011001100", "1100110000000000100110
01", "11001100000000001100110", "1100110000000000110011", "1100110000000000000
00000",
"10011001111111111111111111", "10011001111111111111001100", "10011001111111111100110
01", "10011001111111111101100110", "1001100111111111100110011", "1001100111111111000
00000",
"10011001110011001111111111", "100110011100110011001100", "1001100111001100100110
01", "100110011100110001100110", "100110011100110000110011", "1001100111001100000
00000",
"10011001100110011111111111", "100110011001100111001100", "1001100110011001100110
01", "100110011001100101100110", "100110011001100100110011", "1001100110011001000
00000",
"10011001011001101111111111", "100110010110011011001100", "1001100101100110100110
01", "100110010110011001100110", "100110010110011000110011", "1001100101100110000
00000",
"10011001001100111111111111", "100110010011001111001100", "1001100100110011100110
01", "100110010011001101100110", "100110010011001100110011", "1001100100110011000
00000",
"10011001000000001111111111", "100110010000000011001100", "1001100100000000100110
01", "100110010000000001100110", "10011001000000000110011", "1001100100000000000
00000",
"01100110111111111111111111", "01100110111111111111001100", "01100110111111111100110
01", "01100110111111111101100110", "0110011011111111100110011", "0110011011111111000
00000",
"01100110110011001111111111", "011001101100110011001100", "0110011011001100100110
01", "011001101100110001100110", "011001101100110000110011", "0110011011001100000
00000",
"01100110100110011111111111", "011001101001100111001100", "0110011010011001100110
01", "011001101001100101100110", "011001101001100100110011", "0110011010011001000
00000",
"01100110011001101111111111", "011001100110011011001100", "0110011001100110100110
01", "011001100110011001100110", "011001100110011000110011", "0110011001100110000
00000",
"01100110001100111111111111", "011001100011001111001100", "0110011000110011100110

```
01","011001100011001101100110","011001100011001100110011","0110011000110011000000",
"011001100000000011111111","011001100000000011001100","011001100000000010011001",
"0110011000000000001100110","011001100000000000110011","011001100000000000000000",
"001100111111111111111111","001100111111111111001100","0011001111111111110011001",
"0011001111111111101100110","001100111111111100110011","001100111111111110000000",
"001100111100110011111111","001100111100110011001100","001100111100110010011001",
"001100111100110001100110","001100111100110000110011","0011001111001100000000",
"001100111001100111111111","001100111001100111001100","001100111001100110011001",
"001100111001100101100110","001100111001100100110011","001100111001100100000000",
"001100110110011011111111","001100110110011011001100","001100110110011010011001",
"001100110110011001100110","001100110110011000110011","001100110110011000000000",
"001100110011001111111111","001100110011001111001100","001100110011001110011001",
"001100110011001101100110","001100110011001100110011","001100110011001100000000",
"001100110000000011111111","001100110000000011001100","001100110000000010011001",
"0011001100000000001100110","001100110000000000110011","001100110000000000000000",
"000000001111111111111111","000000001111111111001100","000000001111111110011001",
"0000000011111111101100110","000000001111111100110011","000000001111111110000000",
"000000001100110011111111","000000001100110011001100","000000001100110010011001",
"000000001100110001100110","000000001100110000110011","0000000011001100000000",
"000000001001100111111111","000000001001100111001100","000000001001100110011001",
"000000001001100101100110","000000001001100100110011","000000001001100100000000",
"000000001100110111111111","00000000110011011001100","00000000110011010011001",
"00000000110011001100110","00000000110011000110011","0000000011001100000000",
"000000000110011111111111","00000000011001111001100","00000000011001110011001",
"00000000011001101100110","00000000011001100110011","000000000110011000000000",
"000000000000000011111111","000000000000000011001100","000000000000000010011001",
"0000000000000000001100110","000000000000000000110011","000000000000000000000000",
);
```

```
constant bomb : Array1 :={
```


X"00",X"00",X"2B",X"AD",X"81",X"88",X"B3",X"D7",X"5D",X"08",X"08",X"08",X"08",X"08",X"07",X
"08",X"08",X"08",X"08",X"07",X"08",X"08",X"32",X"5E",X"5E",X"2C",X"07",X"08",X"08",X"08",X"0
8",X"08",X"08",X"07",X"08",X"5D",X"5E",X"57",X"32",X"08",X"07",X"07",X"07",X"08",X"08",X"2C",
X"32",X"33",X"08",X"08",X"08",X"08",X"5E",X"D7",X"AC",X"B2",X"B3",X"B3",X"2C",X"00",
X"00",X"00",X"00",X"32",X"AD",X"AD",X"B3",X"D7",X"5D",X"08",X"08",X"08",X"08",X"08",X"08",X
"08",X"07",X"08",X"08",X"08",X"08",X"08",X"08",X"5E",X"5D",X"07",X"08",X"08",X"08",X"0
8",X"08",X"08",X"07",X"5E",X"5E",X"08",X"08",X"08",X"08",X"08",X"07",X"07",X"08",X"08",X"07",
X"07",X"07",X"08",X"08",X"08",X"08",X"0E",X"AD",X"D7",X"B3",X"D6",X"D7",X"32",X"00",
X"00",X"00",X"00",X"00",X"2B",X"B3",X"D7",X"D7",X"5D",X"08",X"08",X"08",X"08",X"07",X"08",X"
08",X"33",X"33",X"57",X"5D",X"5E",X"5E",X"5D",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08
",X"08",X"08",X"08",X"08",X"33",X"33",X"33",X"33",X"5D",X"32",X"08",X"07",X"08",X"08",X
"08",X"08",X"08",X"08",X"08",X"08",X"5E",X"D7",X"B3",X"D7",X"B3",X"07",X"00",
X"00",X"00",X"00",X"00",X"00",X"07",X"AC",X"D7",X"33",X"08",X"08",X"08",X"07",X"08",X"5D",X"
5D",X"5D",X"B3",X"D7",X"B3",X"57",X"81",X"B3",X"5E",X"2C",X"07",X"08",X"08",X"08",X"08",X"0
8",X"08",X"08",X"07",X"08",X"5E",X"82",X"B3",X"B3",X"AD",X"56",X"88",X"88",X"5D",X"33",X"07"
",X"07",X"08",X"08",X"08",X"08",X"08",X"33",X"D7",X"B2",X"D7",X"88",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"5D",X"33",X"08",X"08",X"07",X"32",X"88",X"57",X"
08",X"08",X"82",X"D7",X"B3",X"88",X"AC",X"33",X"32",X"5E",X"07",X"08",X"08",X"08",X"08",X"08
",X"08",X"08",X"07",X"88",X"33",X"07",X"B3",X"D7",X"B3",X"5D",X"AD",X"57",X"2C",X"5E",X"5E",
X"08",X"08",X"08",X"08",X"08",X"08",X"33",X"B3",X"D7",X"D7",X"2C",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"5D",X"33",X"08",X"08",X"07",X"5D",X"33",X"08",X"
08",X"07",X"08",X"57",X"5D",X"5E",X"5D",X"07",X"08",X"32",X"33",X"57",X"07",X"08",X"08",X"08
",X"08",X"08",X"08",X"5D",X"08",X"07",X"33",X"82",X"88",X"89",X"5D",X"07",X"07",X"08",X"5E",X"
"5D",X"07",X"08",X"08",X"08",X"08",X"33",X"B3",X"D7",X"82",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"5D",X"33",X"08",X"08",X"08",X"08",X"07",X"08",X"
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X"00",X"00",X"00",X"00",X"00",X"00",X"5D",X"33",X"08",X"08",X"08",X"08",X"08",X"08",X"
08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08
",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X
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X"00",X"00",X"00",X"00",X"00",X"5D",X"5D",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"
08",X"08",X"08",X"08",X"08",X"08",X"07",X"08",X"5E",X"08",X"08",X"08",X"08",X"08",X"08
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07",X"5E",X"0F",X"0E",X"0F",X"0E",X"0E",X"0E",X"0F",X"39",X"3A",X"5E",X"5E",X"5E",X"5E",X"5E
",X"5E",X"5E",X"3A",X"0F",X"0E",X"0E",X"0F",X"0F",X"0E",X"33",X"88",X"08",X"08",X"32",X"5E",X,
"07",X"07",X"08",X"08",X"08",X"08",X"5E",X"2B",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"32",X"5D",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"
08",X"57",X"64",X"0E",X"0F",X"0F",X"0F",X"0F",X"0E",X"0E",X"08",X"0E",X"0E",X"0E",X"0E",X"0E
",X"0E",X"0E",X"0E",X"0F",X"0F",X"0F",X"0F",X"0E",X"0F",X"89",X"32",X"08",X"08",X"08",X"08",X
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X"00",X"00",X"00",X"00",X"00",X"00",X"88",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"
08",X"07",X"82",X"39",X"0E",X"0F",X"0E",X"39",X"5E",X"5E",X"5E",X"0F",X"0E",X"0E",X"0E",X"0F
",X"0E",X"0F",X"0F",X"0F",X"0F",X"0E",X"0F",X"88",X"33",X"08",X"08",X"08",X"08",X"08",X
"08",X"08",X"08",X"08",X"08",X"5E",X"2B",X"00",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"88",X"32",X"08",X"08",X"08",X"08",X"08",X"08",X"
08",X"07",X"2C",X"88",X"0F",X"0E",X"5E",X"5D",X"5C",X"38",X"5C",X"88",X"39",X"3A",X"64",X"64
",X"5E",X"0F",X"0E",X"0F",X"0F",X"0E",X"0F",X"89",X"57",X"08",X"08",X"08",X"08",X"08",X
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X"00",X"00",X"00",X"00",X"00",X"00",X"88",X"88",X"08",X"08",X"08",X"08",X"08",X"08",X"
08",X"08",X"08",X"57",X"64",X"3A",X"5D",X"0D",X"0D",X"0D",X"0D",X"38",X"88",X"5D",X"38",X"3
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X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"2B",X"89",X"2C",X"08",X"08",X"08",X"08",X
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0D",X"0D",X"32",X"88",X"0F",X"0F",X"89",X"57",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08
",X"08",X"08",X"0E",X"88",X"2B",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"2B",X"88",X"33",X"08",X"08",X"08",X"
08",X"08",X"08",X"07",X"08",X"82",X"64",X"0D",X"0D",X"0D",X"0D",X"0D",X"0D",X"0D",X"0D",X"0
D",X"0D",X"0D",X"38",X"89",X"64",X"33",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",
X"08",X"0E",X"89",X"2C",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"2B",X"88",X"5D",X"08",X"08",X"
08",X"08",X"08",X"08",X"07",X"08",X"5E",X"88",X"0D",X"0D",X"0D",X"0D",X"0D",X"0D",X"0D",X"0
D",X"0D",X"0D",X"B3",X"88",X"2C",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",
X"0F",X"89",X"56",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"5D",X"5E",X"08",X"
08",X"08",X"08",X"08",X"08",X"07",X"08",X"57",X"88",X"5D",X"38",X"0D",X"0D",X"0D",X"32",X"5
D",X"88",X"88",X"57",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"33",
X"88",X"2C",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"56",X"82",X"
33",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"5D",X"82",X"88",X"88",X"88",X"82
",X"57",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"08",X"5E",X"88",X
"2B",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",
X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"00",X"2B",X"
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);
```

```
signal vga_hblank, vga_hsync,
vga_vblank, vga_vsync : std_logic; -- Sync. signals
```

```
signal rectangle_h, rectangle_v, rectangle, rectangle_h_B, rectangle_v_B, rectangle_B,
rectangle_h_C, rectangle_v_C, rectangle_C,
rectangle_h_E, rectangle_v_E, rectangle_E, rectangle_h_E1, rectangle_v_E1,
rectangle_E1, rectangle_h_E2, rectangle_v_E2, rectangle_E2,
rectangle_h_BM, rectangle_v_BM, rectangle_BM, rectangle_h_LV1, rectangle_v_LV1,
rectangle_LV1, rectangle_h_LV2, rectangle_LV2,
rectangle_h_LV3, rectangle_LV3, rectangle_v_BU, rectangle_h_BU1,
rectangle_BU1, rectangle_h_BU2, rectangle_BU2, rectangle_h_BU3, rectangle_BU3,
rectangle_h_BU4, rectangle_BU4, rectangle_h_BU5, rectangle_BU5, rectangle_h_BOX,
rectangle_v_BOX, rectangle_BOX : std_logic; -- rectangle area
```

```
type ram_type is array(31 downto 0) of
std_logic_vector(15 downto 0);
signal RAM : ram_type:=
1 => "0000000011100000",
14 => "0000000011100000",
2 => "0000000010111000",
13 => "0000000010111000",
3 => "0000000010111000",
19 => "0000000000000000", --BG controller
20 => "0000000101111110", --BOX H
21 => "0000000101111110", --BOX V
```

```
22 => "0000000111111110", --Bullet# 5
23 => "0000000111101010", --Bullet# 4
24 => "0000000111010110", --Bullet# 3
25 => "0000000111000010", --Bullet# 2
26 => "0000000110101110", --Bullet# 1
27 => "0000000101001010", --Lives 3
28 => "0000000100101100", --Lives 2
29 => "0000000100001110", --Lives 1
others=>"0000000000000000");
signal ram_address: unsigned(4 downto 0);
```

```
begin
```

```
ram_address <= unsigned(address(4 downto 0));
```

```
-- Clock handler
```

```
clock_handler : process(clk50)
```

```
begin
```

```
if rising_edge(clk50) then
```

```
clk <= not clk;
```

```
end if;
```

```
end process clock_handler;
```

```
distinguish: process(clk)
```

```
begin
```

```
if rising_edge(clk) then
```

```
if reset_n = '0' then
```

```
mark <= '0';
```

```
else
```

```
mark <= not mark;
```

```
end if;
```

```
end if;
```

```
end process distinguish;
```

```
-- Memory handler
```

```
Memory_handle: process (clk50)
```

```
begin
```

```
if rising_edge(clk50) then
```

```
if reset_n = '0' then
```

```
readdata <= (others => '0');
```

```
else
```

```
if chipselect = '1' then
```

```
if read = '1' then
```

```
readdata <= RAM(conv_integer(ram_address));
```

```
        elsif write = '1' then
            RAM(conv_integer(ram_address)) <= writedata;
        end if;
    end if;
end if;
end if;
end process Memory_handle;
```

-- Horizontal and vertical counters

```
HCounter2 : process (clk)
begin
    if rising_edge(clk) then
        if reset_n = '0' then
            Hcount <= (others => '0');
        elsif EndOfLine = '1' then
            Hcount <= (others => '0');
        else
            Hcount <= Hcount + 1;
        end if;
    end if;
end process HCounter2;
```

```
EndOfLine <= '1' when Hcount = HTOTAL - 1 else '0';
```

```
VCounter2: process (clk)
begin
    if rising_edge(clk) then
        if reset_n = '0' then
            Vcount <= (others => '0');
        elsif EndOfLine = '1' then
            if EndOfField = '1' then
                Vcount <= (others => '0');
            else
                Vcount <= Vcount + 1;
            end if;
        end if;
    end if;
end process VCounter2;
```

```
EndOfField <= '1' when Vcount = VTOTAL - 1 else '0';
```

-- State machines to generate HSYNC, VSYNC, HBLANK, and VBLANK

```
HSyncGen : process (clk)
```

```
begin
  if rising_edge(clk) then
    if reset_n = '0' or EndOfLine = '1' then
      vga_hsync <= '1';
    elsif Hcount = HSYNC - 1 then
      vga_hsync <= '0';
    end if;
  end if;
end process HSyncGen;

HBlankGen : process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      vga_hblank <= '1';
    elsif Hcount = HSYNC + HBACK_PORCH then
      vga_hblank <= '0';
    elsif Hcount = HSYNC + HBACK_PORCH + HACTIVE then
      vga_hblank <= '1';
    end if;
  end if;
end process HBlankGen;

VSyncGen : process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      vga_vsync <= '1';
    elsif EndOfLine = '1' then
      if EndOfField = '1' then
        vga_vsync <= '1';
      elsif Vcount = VSYNC - 1 then
        vga_vsync <= '0';
      end if;
    end if;
  end if;
end process VSyncGen;

VBlankGen : process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      vga_vblank <= '1';
    elsif EndOfLine = '1' then
```



```
    if Vcount = VSYNC + VBACK_PORCH - 1 then
        vga_vblank <= '0';
    elsif Vcount = VSYNC + VBACK_PORCH + VACTIVE - 1 then
        vga_vblank <= '1';
    end if;
end if;
end if;
end process VBlankGen;

-- Rectangle generator Boss
Boss_V : V_control port map (clk, Vcount, PATTERN_V, CONV_INTEGER(RAM(15)), Vcounter,
rectangle_v, reset_n, EndOfLine);
Boss_H : H_control port map (clk, Hcount, PATTERN_H, CONV_INTEGER(RAM(0)), Hcounter,
rectangle_h);

-- Rectangle generator Bullet
Bullet_V : V_control port map (clk, Vcount, PATTERN_V_B, CONV_INTEGER(RAM(14)),
Vcounter_B, rectangle_v_B, reset_n, EndOfLine);
Bullet_H : H_control port map (clk, Hcount, PATTERN_H_B, CONV_INTEGER(RAM(1)),
Hcounter_B, rectangle_h_B);

-- Rectangle generator Student
Student_V : V_control port map (clk, Vcount, PATTERN_V_C, CONV_INTEGER(RAM(13)),
Vcounter_C, rectangle_v_C, reset_n, EndOfLine);
Student_H : H_control port map (clk, Hcount, PATTERN_H_C, CONV_INTEGER(RAM(2)),
Hcounter_C, rectangle_h_C);

-- Rectangle generator Enemy0
Enemy0_V : V_control port map (clk, Vcount, PATTERN_V_E, CONV_INTEGER(RAM(12)),
Vcounter_E, rectangle_v_E, reset_n, EndOfLine);
Enemy0_H : H_control port map (clk, Hcount, PATTERN_H_E, CONV_INTEGER(RAM(3)),
Hcounter_E, rectangle_h_E);

-- Rectangle generator Enemy1
Enemy1_V : V_control port map (clk, Vcount, PATTERN_V_E, CONV_INTEGER(RAM(11)),
Vcounter_E1, rectangle_v_E1, reset_n, EndOfLine);
Enemy1_H : H_control port map (clk, Hcount, PATTERN_H_E, CONV_INTEGER(RAM(4)),
Hcounter_E1, rectangle_h_E1);

-- Rectangle generator Enemy2
Enemy2_V : V_control port map (clk, Vcount, PATTERN_V_E, CONV_INTEGER(RAM(10)),
Vcounter_E2, rectangle_v_E2, reset_n, EndOfLine);
Enemy2_H : H_control port map (clk, Hcount, PATTERN_H_E, CONV_INTEGER(RAM(5)),
Hcounter_E2, rectangle_h_E2);
```

```

-- Rectangle generator Bomb
Bomb_v : V_control port map (clk, Vcount, PATTERN_V_E, CONV_INTEGER(RAM(8)),
Vcounter_BM, rectangle_v_BM, reset_n, EndOfLine);
Bomb_H : H_control port map (clk, Hcount, PATTERN_H_E, CONV_INTEGER(RAM(7)),
Hcounter_BM, rectangle_h_BM);

-- Rectangle generator Lives
LV1_v : V_control port map (clk, Vcount, 30, 70, Vcounter_LV1, rectangle_v_LV1, reset_n,
EndOfLine);
LV1_H : H_control port map (clk, Hcount, 30, CONV_INTEGER(RAM(29)), Hcounter_LV1,
rectangle_h_LV1);
LV2_H : H_control port map (clk, Hcount, 30, CONV_INTEGER(RAM(28)), Hcounter_LV2,
rectangle_h_LV2);
LV3_H : H_control port map (clk, Hcount, 30, CONV_INTEGER(RAM(27)), Hcounter_LV3,
rectangle_h_LV3);

BUN_v : V_control port map (clk, Vcount, 46, 65, Vcounter_BU, rectangle_v_BU, reset_n,
EndOfLine);
BUN1_H : H_control port map (clk, Hcount, 20, CONV_INTEGER(RAM(26)), Hcounter_BU1,
rectangle_h_BU1);
BUN2_H : H_control port map (clk, Hcount, 20, CONV_INTEGER(RAM(25)), Hcounter_BU2,
rectangle_h_BU2);
BUN3_H : H_control port map (clk, Hcount, 20, CONV_INTEGER(RAM(24)), Hcounter_BU3,
rectangle_h_BU3);
BUN4_H : H_control port map (clk, Hcount, 20, CONV_INTEGER(RAM(23)), Hcounter_BU4,
rectangle_h_BU4);
BUN5_H : H_control port map (clk, Hcount, 20, CONV_INTEGER(RAM(22)), Hcounter_BU5,
rectangle_h_BU5);

-- Rectangle generator Box
BOX_v : V_control port map (clk, Vcount, 46, CONV_INTEGER(RAM(21)), Vcounter_BOX,
rectangle_v_BOX, reset_n, EndOfLine);
BOX_H : H_control port map (clk, Hcount, 60, CONV_INTEGER(RAM(20)), Hcounter_BOX,
rectangle_h_BOX);

rectangle <= rectangle_h and rectangle_v;
rectangle_B <= rectangle_h_B and rectangle_v_B;-- and not rectangle;
rectangle_C <= rectangle_h_C and rectangle_v_C;-- and not rectangle and not rectangle_B;
rectangle_BM <= rectangle_h_BM and rectangle_v_BM;-- and not rectangle and not rectangle_B
and not rectangle_C;

rectangle_E <= rectangle_h_E and rectangle_v_E;
rectangle_E1 <= rectangle_h_E1 and rectangle_v_E1;-- and not rectangle_E;

```

```
rectangle_E2 <= rectangle_h_E2 and rectangle_v_E2;-- and not rectangle_E and not rectangle_E1;
```

```
rectangle_LV1 <= rectangle_h_LV1 and rectangle_v_LV1;  
rectangle_LV2 <= rectangle_h_LV2 and rectangle_v_LV1;  
rectangle_LV3 <= rectangle_h_LV3 and rectangle_v_LV1;
```

```
rectangle_BU1 <= rectangle_h_BU1 and rectangle_v_BU;  
rectangle_BU2 <= rectangle_h_BU2 and rectangle_v_BU;  
rectangle_BU3 <= rectangle_h_BU3 and rectangle_v_BU;  
rectangle_BU4 <= rectangle_h_BU4 and rectangle_v_BU;  
rectangle_BU5 <= rectangle_h_BU5 and rectangle_v_BU;
```

```
rectangle_BOX <= rectangle_h_BOX and rectangle_v_BOX;
```

```
process (clk)  
variable index1 : integer :=0;  
variable index8 : integer :=0;  
begin  
if clk'event and clk = '1' then  
    index1 := Vcounter*PATTERN_H+Hcounter;  
    if CONV_INTEGER(ram(30)) = 2 then  
        cmpindex1 <= CONV_INTEGER(pattern3(index1));  
    elsif CONV_INTEGER(ram(30)) = 1 then  
        cmpindex1 <= CONV_INTEGER(pattern2(index1));  
    else  
        cmpindex1 <= CONV_INTEGER(pattern(index1));  
    end if;  
    index8 := Vcounter_BM*PATTERN_H_E+Hcounter_BM;  
    cmpindex8 <=CONV_INTEGER(bomb(index8));  
end if;  
end process;
```

```
process (clk)  
variable indexBU1 : integer :=0;  
variable indexBU2 : integer :=0;  
variable indexBU3 : integer :=0;  
variable indexBU4 : integer :=0;  
variable indexBU5 : integer :=0;  
begin  
if clk'event and clk = '1' then  
    indexBU1 := Vcounter_BU*20+Hcounter_BU1;  
    cmpindexBU1 <=CONV_INTEGER(BUN(indexBU1));  
    indexBU2 := Vcounter_BU*20+Hcounter_BU2;  
    cmpindexBU2 <=CONV_INTEGER(BUN(indexBU2));
```

```

indexBU3 := Vcounter_BU*20+Hcounter_BU3;
cmpindexBU3 <=CONV_INTEGER(BUN(indexBU3));
indexBU4 := Vcounter_BU*20+Hcounter_BU4;
cmpindexBU4 <=CONV_INTEGER(BUN(indexBU4));
indexBU5 := Vcounter_BU*20+Hcounter_BU5;
cmpindexBU5 <=CONV_INTEGER(BUN(indexBU5));
end if;
end process;

RGB3 : process (clk)
variable colorindex : std_logic_vector(23 downto 0);
begin
if clk'event and clk = '1' then
  if rectangle = '1' and not (cmpindex1=0) then
    colorindex := colormap(cmpindex1);
    LEVEL_3_R(9 downto 2) <=colorindex(23 downto 16);
    LEVEL_3_G(9 downto 2) <=colorindex(15 downto 8);
    LEVEL_3_B(9 downto 2) <=colorindex(7 downto 0);
    level_3 <= '1';
  elsif rectangle_BM = '1' and not (cmpindex8=0)then
    colorindex := colormap(cmpindex8);
    LEVEL_3_R(9 downto 2)<=colorindex(23 downto 16);
    LEVEL_3_G(9 downto 2)<=colorindex(15 downto 8);
    LEVEL_3_B(9 downto 2)<=colorindex(7 downto 0);
    level_3 <= '1';
  elsif rectangle_BU1 = '1' and not (cmpindexBU1=0) then
    colorindex := colormap(cmpindexBU1);
    LEVEL_3_R(9 downto 2)<=colorindex(23 downto 16);
    LEVEL_3_G(9 downto 2)<=colorindex(15 downto 8);
    LEVEL_3_B(9 downto 2)<=colorindex(7 downto 0);
    level_3 <= '1';
  elsif rectangle_BU2 = '1' and not (cmpindexBU2=0) then
    colorindex := colormap(cmpindexBU2);
    LEVEL_3_R(9 downto 2)<=colorindex(23 downto 16);
    LEVEL_3_G(9 downto 2)<=colorindex(15 downto 8);
    LEVEL_3_B(9 downto 2)<=colorindex(7 downto 0);
    level_3 <= '1';
  elsif rectangle_BU3 = '1' and not (cmpindexBU3=0) then
    colorindex := colormap(cmpindexBU3);
    LEVEL_3_R(9 downto 2)<=colorindex(23 downto 16);
    LEVEL_3_G(9 downto 2)<=colorindex(15 downto 8);
    LEVEL_3_B(9 downto 2)<=colorindex(7 downto 0);
    level_3 <= '1';
  elsif rectangle_BU4 = '1' and not (cmpindexBU4=0) then

```

```
        colorindex := colormap(cmpindexBU4);
        LEVEL_3_R(9 downto 2) <= colorindex(23 downto 16);
        LEVEL_3_G(9 downto 2) <= colorindex(15 downto 8);
        LEVEL_3_B(9 downto 2) <= colorindex(7 downto 0);
        level_3 <= '1';
    elsif rectangle_BU5 = '1' and not (cmpindexBU5=0) then
        colorindex := colormap(cmpindexBU5);
        LEVEL_3_R(9 downto 2) <= colorindex(23 downto 16);
        LEVEL_3_G(9 downto 2) <= colorindex(15 downto 8);
        LEVEL_3_B(9 downto 2) <= colorindex(7 downto 0);
        level_3 <= '1';
    else
        level_3 <= '0';
    end if;
end if;
end process RGB3;
```

```
process (clk)
variable index2 : integer :=0;
variable index3 : integer :=0;
begin
if clk'event and clk = '1' then
    index2 := Vcounter_B*PATTERN_H_B+Hcounter_B;
    cmpindex2 <= CONV_INTEGER(B1(index2));
    index3 := Vcounter_C*PATTERN_H_C+Hcounter_C;
    if CONV_INTEGER(ram(31))=0 then
        cmpindex3 <= CONV_INTEGER(C1(index3));
    else
        cmpindex3 <= CONV_INTEGER(C2(index3));
    end if;
end if;
end process;
```

```
process (clk)
variable index4 : integer :=0;
variable index5 : integer :=0;
variable index6 : integer :=0;
variable indexLV1 : integer :=0;
variable indexLV2 : integer :=0;
variable indexLV3 : integer :=0;
variable indexBOX : integer :=0;
begin
if clk'event and clk = '1' then
    index4 := Vcounter_E*PATTERN_H_E+Hcounter_E;
```

```

    cmpindex4 <= CONV_INTEGER(E1(index4));
    index5 := Vcounter_E1*PATTERN_H_E+Hcounter_E1;
    cmpindex5 <= CONV_INTEGER(E1(index5));
    index6 := Vcounter_E2*PATTERN_H_E+Hcounter_E2;
    cmpindex6 <= CONV_INTEGER(E1(index6));
    indexLV1 := Vcounter_LV1*30+Hcounter_LV1;
    cmpindexLV1 <= CONV_INTEGER(lives(indexLV1));
    indexLV2 := Vcounter_LV1*30+Hcounter_LV2;
    cmpindexLV2 <= CONV_INTEGER(lives(indexLV2));
    indexLV3 := Vcounter_LV1*30+Hcounter_LV3;
    cmpindexLV3 <= CONV_INTEGER(lives(indexLV3));
    indexBOX := Vcounter_BOX*60+Hcounter_BOX;
    cmpindexBOX <= CONV_INTEGER(BOX(indexBOX));
end if;
end process;

RGB2 : process (clk)
variable colorindex : std_logic_vector(23 downto 0);
begin
if clk'event and clk = '1' then
    if rectangle_B = '1' and (not (cmpindex2=0))then
        colorindex := colormap(cmpindex2);
        LEVEL_2_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_2_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_2_B(9 downto 2)<=colorindex(7 downto 0);
        level_2 <= '1';
    elsif rectangle_C = '1' and (not (cmpindex3=0))then
        colorindex := colormap(cmpindex3);
        LEVEL_2_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_2_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_2_B(9 downto 2)<=colorindex(7 downto 0);
        level_2 <= '1';
    elsif rectangle_LV1 = '1' and not (cmpindexLV1=0) then
        colorindex := colormap(cmpindexLV1);
        LEVEL_2_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_2_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_2_B(9 downto 2)<=colorindex(7 downto 0);
        level_2 <= '1';
    elsif rectangle_LV2 = '1' and not (cmpindexLV2=0) then
        colorindex := colormap(cmpindexLV2);
        LEVEL_2_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_2_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_2_B(9 downto 2)<=colorindex(7 downto 0);
        level_2 <= '1';

```

```
    elsif rectangle_LV3 = '1' and not (cmpindexLV3=0) then
        colorindex := colormap(cmpindexLV3);
        LEVEL_2_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_2_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_2_B(9 downto 2)<=colorindex(7 downto 0);
        level_2 <= '1';
    else
        level_2 <= '0';
    end if;
end if;
end process RGB2;
```

```
RGB1 : process (clk)
variable colorindex : std_logic_vector(23 downto 0);
begin
if clk'event and clk = '1' then
    if rectangle_E = '1' and not (cmpindex4=0) then
        colorindex := colormap(cmpindex4);
        LEVEL_1_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_1_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_1_B(9 downto 2)<=colorindex(7 downto 0);
        level_1 <= '1';
    elsif rectangle_E1 ='1' and not (cmpindex5=0) then
        colorindex := colormap(cmpindex5);
        LEVEL_1_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_1_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_1_B(9 downto 2)<=colorindex(7 downto 0);
        level_1 <= '1';
    elsif rectangle_E2 ='1' and not (cmpindex6=0)then
        colorindex := colormap(cmpindex6);
        LEVEL_1_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_1_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_1_B(9 downto 2)<=colorindex(7 downto 0);
        level_1 <= '1';
    elsif rectangle_BOX ='1' and not (cmpindexBOX=0)then
        colorindex := colormap(cmpindexBOX);
        LEVEL_1_R(9 downto 2)<=colorindex(23 downto 16);
        LEVEL_1_G(9 downto 2)<=colorindex(15 downto 8);
        LEVEL_1_B(9 downto 2)<=colorindex(7 downto 0);
        level_1 <= '1';
    else
        level_1 <= '0';
    end if;
end if;
end if;
```

```
end process RGB1;
```

```
RGB0 : process (clk)
variable cmpindexBG : integer :=0;
variable colorindex : std_logic_vector(23 downto 0);
begin
if clk'event and clk = '1' then
    if mark = '0' then
        cmpindexBG := conv_integer(sram_read(15 downto 8));
    elsif mark = '1' then
        cmpindexBG := conv_integer(sram_read(7 downto 0));
    end if;
    colorindex := colormap(cmpindexBG);
    level_0_R(9 downto 2) <= colorindex(23 downto 16);
    level_0_G(9 downto 2) <= colorindex(15 downto 8);
    level_0_B(9 downto 2) <= colorindex(7 downto 0);
end if;
end process RGB0;
```

```
-- Registered video signals going to the video DAC
```

```
VideoOut: process (reset_n, clk)
begin
    if reset_n = '0' then
        VGA_R <= "0000000000";
        VGA_G <= "0000000000";
        VGA_B <= "0000000000";
    elsif clk'event and clk = '1' then
        if level_3 = '1' then
            VGA_R <= LEVEL_3_R;
            VGA_G <= LEVEL_3_G;
            VGA_B <= LEVEL_3_B;
        elsif level_2 = '1' then
            VGA_R <= LEVEL_2_R;
            VGA_G <= LEVEL_2_G;
            VGA_B <= LEVEL_2_B;
        elsif level_1 = '1' then
            VGA_R <= LEVEL_1_R;
            VGA_G <= LEVEL_1_G;
            VGA_B <= LEVEL_1_B;
        elsif vga_hblank = '0' and vga_vblank = '0' then
```



```

        VGA_R <= LEVEL_0_R;
        VGA_G <= LEVEL_0_G;
        VGA_B <= LEVEL_0_B;
    else
        VGA_R <= "0000000000";
        VGA_G <= "0000000000";
        VGA_B <= "0000000000";
    end if;
end if;
end process VideoOut;

VGA_CLK <= clk;
VGA_HS <= not vga_hsync;
VGA_VS <= not vga_vsync;
VGA_SYNC <= '0';
VGA_BLANK <= not (vga_hsync or vga_vsync);
hcounter_s <= conv_integer(Hcount);
vcounter_s <= conv_integer(Vcount);

process (clk)
begin
    if rising_edge(clk) then
        if reset_n = '0' then
            sram_add <= (others => '0');
        elsif CONV_INTEGER(RAM(19))=1 and hcounter_s<450+HSYNC+HBACK_PORCH-1 and
hcounter_s>150+HSYNC+HBACK_PORCH-1 and vcounter_s<430+VSYNC+VBACK_PORCH-1 and
vcounter_s>330+VSYNC+VBACK_PORCH-1 then
            sram_add <=Conv_std_logic_vector((hcounter_s - HSYNC -
HBACK_PORCH-150)/2+ (vcounter_s-VSYNC-VBACK_PORCH-330)*150+153600 ,18);

        elsif CONV_INTEGER(RAM(19))=2 and hcounter_s<350+HSYNC+HBACK_PORCH-1 and
hcounter_s>200+HSYNC+HBACK_PORCH-1 and vcounter_s<430+VSYNC+VBACK_PORCH-1 and
vcounter_s>330+VSYNC+VBACK_PORCH-1 then
            sram_add <=Conv_std_logic_vector((hcounter_s - HSYNC -
HBACK_PORCH-200)/2+ (vcounter_s-VSYNC-VBACK_PORCH-330)*75+168600 ,18);

        elsif CONV_INTEGER(RAM(19))=3 and hcounter_s<350+HSYNC+HBACK_PORCH-1 and
hcounter_s>200+HSYNC+HBACK_PORCH-1 and vcounter_s<430+VSYNC+VBACK_PORCH-1 and
vcounter_s>330+VSYNC+VBACK_PORCH-1 then
            sram_add <=Conv_std_logic_vector((hcounter_s - HSYNC -
HBACK_PORCH-200)/2+ (vcounter_s-VSYNC-VBACK_PORCH-330)*75+176100 ,18);

        elsif CONV_INTEGER(RAM(19))=4 and hcounter_s<350+HSYNC+HBACK_PORCH-1 and
hcounter_s>200+HSYNC+HBACK_PORCH-1 and vcounter_s<430+VSYNC+VBACK_PORCH-1 and

```

```

vcounter_s>330+VSYNC+VBACK_PORCH-1 then
    sram_add    <=Conv_std_logic_vector((hcounter_s    -    HSYNC    -
HBACK_PORCH-200)/2+ (vcounter_s-VSYNC-VBACK_PORCH-330)*75+183600 ,18);

    elsif CONV_INTEGER(RAM(19))=0 and hcounter_s<260+HSYNC+HBACK_PORCH-1 and
hcounter_s>200+HSYNC+HBACK_PORCH-1 and vcounter_s<470+VSYNC+VBACK_PORCH-1 and
vcounter_s>440+VSYNC+VBACK_PORCH-1 then
        sram_add    <=Conv_std_logic_vector((hcounter_s    -    HSYNC    -
HBACK_PORCH-200)/2+ (vcounter_s-VSYNC-VBACK_PORCH-440)*30+193500 ,18);

        elsif CONV_INTEGER(RAM(19))=0 and hcounter_s<276+HSYNC+HBACK_PORCH-1 and
hcounter_s>260+HSYNC+HBACK_PORCH-1 and vcounter_s<470+VSYNC+VBACK_PORCH-1 and
vcounter_s>440+VSYNC+VBACK_PORCH-1 then
            sram_add    <=Conv_std_logic_vector((hcounter_s    -    HSYNC    -
HBACK_PORCH-260)/2+
(vcounter_s-VSYNC-VBACK_PORCH-440)*8+191100+CONV_INTEGER(RAM(9))*240 ,18);

            elsif CONV_INTEGER(RAM(19))=0 and hcounter_s<292+HSYNC+HBACK_PORCH-1 and
hcounter_s>276+HSYNC+HBACK_PORCH-1 and vcounter_s<470+VSYNC+VBACK_PORCH-1 and
vcounter_s>440+VSYNC+VBACK_PORCH-1 then
                sram_add    <=Conv_std_logic_vector((hcounter_s    -    HSYNC    -
HBACK_PORCH-276)/2+
(vcounter_s-VSYNC-VBACK_PORCH-440)*8+191100+CONV_INTEGER(RAM(16))*240 ,18);

                elsif CONV_INTEGER(RAM(19))=0 and hcounter_s<308+HSYNC+HBACK_PORCH-1 and
hcounter_s>292+HSYNC+HBACK_PORCH-1 and vcounter_s<470+VSYNC+VBACK_PORCH-1 and
vcounter_s>440+VSYNC+VBACK_PORCH-1 then
                    sram_add    <=Conv_std_logic_vector((hcounter_s    -    HSYNC    -
HBACK_PORCH-292)/2+
(vcounter_s-VSYNC-VBACK_PORCH-440)*8+191100+CONV_INTEGER(RAM(17))*240 ,18);

                    elsif CONV_INTEGER(RAM(19))=0 and hcounter_s<324+HSYNC+HBACK_PORCH-1 and
hcounter_s>308+HSYNC+HBACK_PORCH-1 and vcounter_s<470+VSYNC+VBACK_PORCH-1 and
vcounter_s>440+VSYNC+VBACK_PORCH-1 then
                        sram_add    <=Conv_std_logic_vector((hcounter_s    -    HSYNC    -
HBACK_PORCH-308)/2+
(vcounter_s-VSYNC-VBACK_PORCH-440)*8+191100+CONV_INTEGER(RAM(18))*240 ,18);

                        else
                            sram_add <=Conv_std_logic_vector((hcounter_s - HSYNC - HBACK_PORCH)/2+
(vcounter_s-VSYNC-VBACK_PORCH-1)*320 ,18);
                        end if;

```

```
    end if;
end process;

end rtl;
```

de2_led_controller.vhd

--Build it with VGA top in SOPC

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;
use ieee.std_logic_arith.all;

entity de2_led_controller is
    port (
        clk : in std_logic;
        reset_n : in std_logic;
        read : in std_logic;
        write : in std_logic;
        chipselect : in std_logic;
        address : in std_logic_vector(4 downto 0);
        readdata : out std_logic_vector(15 downto 0);
        writedata : in std_logic_vector(15 downto 0);
        HEX0, HEX1, HEX2, HEX3 : out std_logic_vector(6 downto 0)
    );
end de2_led_controller;

architecture rtl of de2_led_controller is
    type ram_type is array(3 downto 0) of std_logic_vector(15 downto 0);
    signal RAM : ram_type;
    signal ram_address : unsigned(3 downto 0);

    component decoder
    port(
        sel:in integer;
        res:out std_logic_vector(6 downto 0)
    );
    end component;

begin
    ram_address <= unsigned(address(3 downto 0));
    Digital0: decoder port map(CONV_INTEGER(RAM(0)), HEX0);
```

```

Digital1: decoder port map(CONV_INTEGER(RAM(1)), HEX1);
Digital2: decoder port map(CONV_INTEGER(RAM(2)), HEX2);
Digital3: decoder port map(CONV_INTEGER(RAM(3)), HEX3);
process (clk)
begin
  if rising_edge(clk) then
    if reset_n = '0' then
      --      HEX0 <= (others => '0');
      --      HEX1 <= (others => '0');
      --      HEX2 <= (others => '0');
      --      HEX3 <= (others => '0');
    else
      if chipselect = '1' then
        if read = '1' then
          readdata <= RAM(CONV_INTEGER(ram_address));
        elsif write = '1' then
          RAM(CONV_INTEGER(ram_address)) <= writedata;
        end if;
      end if;
    end if;
  end if;
end process;
end rtl;

```

V_control.vhd

--Build it with VGA top in SOPC

```

library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

```

entity V_control is

```

port(
  clk      :    in std_logic;
  Vcount   :    in unsigned(9 downto 0);

  Pattern_V:    in  integer;
  locate   :    in  integer;
  Vcounter :    buffer integer;

```

```
        flag_v    :    out  std_logic;
        reset_n   :    in   std_logic;
        EndofLine:    in   std_logic
    );
end entity V_control;

architecture rtl of V_control is
    constant VSYNC      : integer := 2;
    constant VBACK_PORCH : integer := 33;
begin
    process(clk)
    begin
        if rising_edge(clk) then
            if reset_n = '0' then
                flag_v <= '0';
            elsif EndofLine = '1' then
                if Vcount < VSYNC + VBACK_PORCH - 1 + locate then
                    flag_v <= '0';
                elsif Vcount = VSYNC + VBACK_PORCH - 1 + locate then
                    flag_v <= '1';
                    Vcounter <= 0;
                elsif Vcount > VSYNC + VBACK_PORCH - 1 + locate and Vcount < VSYNC +
VBACK_PORCH - 1 + locate + Pattern_V then
                    Vcounter <= Vcounter + 1;
                elsif Vcount >= VSYNC + VBACK_PORCH - 1 + locate + Pattern_V then
                    Vcounter <= 0;
                    flag_v <= '0';
                end if;
            end if;
        end if;
    end process;
end rtl;
```

decoder.vhd

--Build it with Led controller

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
```

```
entity decoder is
port(
    sel:in integer;
    res:out std_logic_vector(6 downto 0)
);
end decoder;
```

```
architecture imp of decoder is
begin
    res<="1000000" when sel=0 else
        "1111001" when sel=1 else
        "0100100" when sel=2 else
        "0110000" when sel=3 else
        "0011001" when sel=4 else
        "0010010" when sel=5 else
        "0000010" when sel=6 else
        "1111000" when sel=7 else
        "0000000" when sel=8 else
        "0010000" when sel=9 else
        (others => 'X');
end imp;
```

Hello_world.c, our main project software

```
#include <io.h>
#include <system.h>
#include <stdio.h>
#include <time.h>

#include "back.h"
/*
 * sram distribution
 * (31) 0,1 for differnt face (2,13) for player
 * (3,12) (4,11) (5,10) for enemies
 * (30) 0,1,2 for different face (0,15) for boss
 * (1,14) for bullet
 * (7,8) for firework
 * 19 -- 0 normal --1 begin -- 2 A -- 3 B -- C 4
 * 9 16 17 18 score from thousand
 * 27 28 29 for lifes
 * 20 21 for box
 */
```

```

*/
#define IOWR_SRAM_DATA(base, offset, data) \
    IOWR_16DIRECT(base, (offset) * 2, data)
#define IORD_SRAM_DATA(base, offset) \
    IORD_16DIRECT(base, (offset) * 2)

int vadd = 0;
void newBackGroundMusic ()
{
    int i = 1;
    while (i < 32){
        IOWR_16DIRECT (AUDIO_BASE, i*2 , value[vadd]);
        vadd++;
        if (vadd >= 131805){
            vadd = 0;
        }
        i++;
    }
}

int main()
{
    ////////////////////////////////////////////////////////////////////
    //every time want to use the sound effect :piu , use the following two
    //sentences together;
    //          //Sound for dead:
    //    IOWR_16DIRECT (AUDIO_BASE, 0 , 1);
    //    IOWR_16DIRECT (AUDIO_BASE, 0 , 2);
    //
    //          //Sound for hitting:
    //    IOWR_16DIRECT (AUDIO_BASE, 0 , 3);
    //    IOWR_16DIRECT (AUDIO_BASE, 0 , 4);
    //
    //          //Sound for laughing:
    //    IOWR_16DIRECT (AUDIO_BASE, 0 , 5);
    //    IOWR_16DIRECT (AUDIO_BASE, 0 , 6);
    ////////////////////////////////////////////////////////////////////

    alt_irq_register(AUDIO_IRQ, NULL, (void*)newBackGroundMusic );
    //define all the variable

```

```
int flag = 0;    // use to determine what state we are

int gameTime = 0;    // time count
int score = 0;    // score count
int finalScore = 0;

int deadFlag;    //indicates player has been created
int playerXCoordinate;    //player's leftmost upmost coordinate
int playerYCoordinate;
int life;    //indicate how many life still left
int openMouthTime;    //time period for open mouth animation

int bossFlag;    //indicates boss has been created
int bossXCoordinate; //boss's leftmost upmost coordinate
int bossYCoordinate;
int bossLife;    //indicate how many life boss still left

int enemyCount; // number of enemies in the screen up to 8 enemies
int enemyFlag[9]; //indicate whethor enemy exists max to 10
int enemyXCoordinate[9]; //enemies' leftmost upmost coordinate
int enemyYCoordinate[9];
int fireworkTime; //time period for firework animation

int bulletFlag; //indicate bullet created
int bulletXCoordinate; //bullet leftmost upmost coordinate
int bulletYCoordinate;
int bulletNumber;

int boxFlag;    //indicate box created
int boxXCoordinate;
int boxYCoordinate;

int playerXSpeed; //speed for everything
int playerYSpeed;
int enemyXSpeed;
int enemyYSpeed;
int bossXSpeed;
int bossYSpeed;
int bulletXSpeed;
int boxXSpeed;

int xLowBound = 0;    // bound for the screen pixels
int xHighBound = 640;
int yLowBound = 0;
```



```
int yHighBound = 480;

int counterTime; // raise the clock to make a loop longer
int counterFly;
int counterDrop;
int counterNormal;
int shine =0; // variable for dead effect

IOWR_SRAM_DATA(VGA_BASE,19,1); // init begin display

//init display all out the screen
IOWR_SRAM_DATA(VGA_BASE,0,800);
IOWR_SRAM_DATA(VGA_BASE,1,800);
IOWR_SRAM_DATA(VGA_BASE,2,800);
IOWR_SRAM_DATA(VGA_BASE,3,800);
IOWR_SRAM_DATA(VGA_BASE,4,800);
IOWR_SRAM_DATA(VGA_BASE,5,800);
IOWR_SRAM_DATA(VGA_BASE,7,800);
IOWR_SRAM_DATA(VGA_BASE,20, 800);
IOWR_SRAM_DATA(VGA_BASE,9,0);
IOWR_SRAM_DATA(VGA_BASE,16,0);
IOWR_SRAM_DATA(VGA_BASE,17,0);
IOWR_SRAM_DATA(VGA_BASE,18,0);
IOWR_SRAM_DATA(LED_BASE, 0, 0);
IOWR_SRAM_DATA(LED_BASE, 1, 0);
IOWR_SRAM_DATA(LED_BASE, 2, 0);
IOWR_SRAM_DATA(LED_BASE, 3, 0);

int startFlag = 0;
while(IORD_SRAM_DATA(VGA_BASE, 19) != 0){
    int beginSound = IORD_16DIRECT(AUDIOSLAVE_BASE,0);
    if( beginSound < 20000 || beginSound >46535 || (beginSound>32000 && beginSound<
33000)){
        // threshold move up 1000
        startFlag = 0;
    }else{
        startFlag++;
        if(startFlag > 25){
            startFlag = 0;
            IOWR_SRAM_DATA(VGA_BASE,19,0);
        }
    }
}
```

```
}

playerXCoordinate = 40;    // init positions
playerYCoordinate = 360;
bossXCoordinate = 550;
bossYCoordinate = 400;
bulletXCoordinate = 600;
bulletYCoordinate = 480;
boxXCoordinate = 800;
boxYCoordinate = 800;

playerYSpeed = 1; //init speeds
enemyXSpeed = 1;
bossXSpeed = 0;
bossYSpeed = 0;
bulletXSpeed = 4;
boxXSpeed = 2;

deadFlag = 0; //int flags
bossFlag = 0;
bulletFlag = 0;
boxFlag = 0;
life = 3; //init lifes
bulletNumber = 5;

int i = 0; //init for enemyflags
int j = 0;
for(i = 0; i < 10; i++){
    enemyFlag[i] = 0;
    enemyXCoordinate[i] = 800;
    enemyYCoordinate[i] = 800;
}
enemyCount = 0;

counterTime = 500;    //init counters
counterDrop = 500;
counterFly = 500;
counterNormal = 500;

srand(time(NULL));    //init rand seed

IOWR_SRAM_DATA(VGA_BASE,31, 0); // init player and boss initial faces
IOWR_SRAM_DATA(VGA_BASE,30, 0);
```

```
openMouthTime = 0; //init animation time
fireworkTime = 0;

for (;){
    ///printf("dfsadfsdfsad");
    // get sound from avalon bus
    int sound = IORD_16DIRECT(AUDIOSLAVE_BASE,0);

    counterTime--;
    //simulate real time
    if(counterTime == 0){
        counterTime = 50000; //215000 times the clock time
        gameTime = gameTime + 1;
        score = score + 2;
        if(score > 9999){
            score = 9999;
        }
        if(gameTime%10 == 0){
            //printf("%d seconds since game starts \n", gameTime);
        }

        IOWR_SRAM_DATA(LED_BASE, 0, score%10);
        IOWR_SRAM_DATA(LED_BASE, 1, (score%100)/10);
        IOWR_SRAM_DATA(LED_BASE, 2, (score%1000)/100);
        IOWR_SRAM_DATA(LED_BASE, 3, score/1000);

        IOWR_SRAM_DATA(VGA_BASE, 18, score%10);
        IOWR_SRAM_DATA(VGA_BASE, 17, (score%100)/10);
        IOWR_SRAM_DATA(VGA_BASE, 16, (score%1000)/100);
        IOWR_SRAM_DATA(VGA_BASE, 9, score/1000);
        // vga score
    }

    //main function
    if( sound < 1700 || sound > 64235 || (sound > 32000 && sound < 33000)){
        // no sound input case
        counterDrop--;
        //counterFly = 10000; //problem
        if(counterDrop == 0){
            counterDrop = 500;
            if(flag > 4 && flag <= 13){
```

```

// warning flag is now between 4 to 10
// shot case
flag = 0; //problem
//printf("shot at %d ----- \n", playerYCoordinate);

// create bullet
if(bulletFlag == 0 && bulletNumber > 0){
    bulletXCoordinate = 70;
    bulletYCoordinate = playerYCoordinate + 50;
    bulletFlag = 1;
    bulletNumber = bulletNumber - 1;
}
//open mouth
IOWR_SRAM_DATA(VGA_BASE,31, 1);
openMouthTime = gameTime;
}else{
// drop case
flag = 0; //problem
////printf("drop >>>>>>>>>>>>>>>>>>>>>>>>>\n");

//player moving ---- drop
playerYSpeed = 1;
if(yHighBound - playerYCoordinate >= 90){
    playerYCoordinate = playerYCoordinate + playerYSpeed;
}
}
}

}else{
//got sound input case = fly case
counterFly--;
counterDrop = 500; //problem
if(counterFly == 0){
    ///printf("fly <<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<<\n");
    counterFly = 500;
    flag = flag + 1;

    //printf("%d!!!!!!!!!!!!!!!!!!!!\n", flag);
    //player moving ---- fly
    playerYSpeed = -3;
    if( (sound > 10000 && sound <30000) || (sound <55535 && sound>35535 )){
        playerYSpeed = -10;
    }
    if(playerYCoordinate - yLowBound >= 100){

```

```

        playerYCoordinate = playerYCoordinate + playerYSpeed;
    }
}

counterNormal--;
if(counterNormal == 0){
    //usual event
    counterNormal = 500;

    //shine and super mode after dead
    if(deadFlag == 1){
        if(shine == 10 || shine == 20 || shine == 30 || shine == 40 || shine == 50 ||
shine == 60 || shine == 70 || shine == 80 || shine == 90 ){
            IOWR_SRAM_DATA(VGA_BASE, 2, 800);
            IOWR_SRAM_DATA(VGA_BASE, 13, 800);
            shine = shine + 1;
        }else if(shine == 100){
            IOWR_SRAM_DATA(VGA_BASE, 2, 800);
            IOWR_SRAM_DATA(VGA_BASE, 13, 800);
            deadFlag = 0;
            shine = 0;
            //printf("super mode over \n");
        }else{

            IOWR_SRAM_DATA(VGA_BASE, 2, playerXCoordinate);
            IOWR_SRAM_DATA(VGA_BASE, 13, playerYCoordinate);
            shine = shine + 1;
        }
    }else{
        IOWR_SRAM_DATA(VGA_BASE, 2, playerXCoordinate);
        IOWR_SRAM_DATA(VGA_BASE, 13, playerYCoordinate);
    }

    //enemy created
    int randNumberSeed = rand()%1000;
    int randNumber = randNumberSeed%100;
    if(randNumber > 97 && enemyCount < 3){
        //rand is from 0-99, thus 0.01% runs created enemy
        //create enemy of No.(enemyCount + 1)
        i = 0;
        //find the empty flag

```

```

while(enemyFlag[i] == 1 && i<5){
    i++;
}
//assign random position
enemyXCoordinate[i] = 620;
enemyYCoordinate[i] = (randNumberSeed/3) + 10;

//
if( enemyYCoordinate[i] >= 100){
    enemyFlag[i] = 1;
    //make sure enemy don't overlap for hardware
    for(j=0; j< i; j++){
        if(abs(enemyYCoordinate[i] - enemyYCoordinate[j]) <= 80 &&
abs(enemyXCoordinate[i] - enemyXCoordinate[j] <= 60)){
            enemyFlag[i] = 0;
        }
    }
    if(i < 3){
        for(j=i+1; j< 3; j++){
            if(abs(enemyYCoordinate[i] - enemyYCoordinate[j]) <= 80 &&
abs(enemyXCoordinate[i] - enemyXCoordinate[j] <= 60)){
                enemyFlag[i] = 0;
            }
        }
    }
    if(enemyFlag[i] == 1){
        enemyCount++;
        //printf("an enemy emerge at %d, there are %d enemies
\n",enemyYCoordinate[i], enemyCount + 1);
    }
}
}

```

```

//enemy engaging
for(i = 0; i < 3; i++){
    if(enemyFlag[i] == 1){
        enemyXCoordinate[i] = enemyXCoordinate[i] - enemyXSpeed;
        if(enemyXCoordinate[i] < 19){
            enemyFlag[i] = 0;
            enemyCount --;
            IOWR_SRAM_DATA(VGA_BASE, 3+i , 800);
            IOWR_SRAM_DATA(VGA_BASE,12-i, 800);
            //printf("an enemy passed, there are %d enemies \n", enemyCount

```

```

+ 1);
        }else{
            IOWR_SRAM_DATA(VGA_BASE,3+i, enemyXCoordinate[i]);
            IOWR_SRAM_DATA(VGA_BASE,12-i, enemyYCoordinate[i]);
        }
    }
}

```

```

//boss created
if(gameTime > 1 && gameTime < 3 && bossFlag == 0){
    //create boss only between a time
    bossFlag = 1;
    //printf("boss created \n");
    bossLife = 1000;
    //assign init position
    bossXCoordinate = 550;
    bossYCoordinate = 400;
    // first face
    IOWR_SRAM_DATA(VGA_BASE,30, 0);
    IOWR_SRAM_DATA(VGA_BASE, 0, 550);
    IOWR_SRAM_DATA(VGA_BASE, 15, 400);
}
if(gameTime > 25 && gameTime < 35){
    // second face
    IOWR_SRAM_DATA(VGA_BASE,30, 1);
}

if(gameTime > 35 && gameTime < 37){
    //third face and move
    IOWR_SRAM_DATA(VGA_BASE,30, 2);
    bossYSpeed = -2;
    bossXSpeed = 1;
    bossLife = 3;
    //IOWR_16DIRECT (AUDIO_BASE, 0 , 5);
    //IOWR_16DIRECT (AUDIO_BASE, 0 , 6);
}
//boss engaging
if(bossFlag == 1){
    if(bossYCoordinate - yLowBound <= 100){
        bossYSpeed = -bossYSpeed;
    }
    if(yHighBound - bossYCoordinate <= 79){

```

```
        bossYSpeed = -bossYSpeed;
    }
    bossXCoordinate = bossXCoordinate - bossXSpeed;
    bossYCoordinate = bossYCoordinate + bossYSpeed;
    if(bossXCoordinate < 20){
        bossFlag = 0;
        //printf("boss passed \n");
        IOWR_SRAM_DATA(VGA_BASE, 0, 800);
        IOWR_SRAM_DATA(VGA_BASE, 15, 800);
        bossXCoordinate = 550;
        bossYCoordinate = 400;
    }else{
        //give it to hardware
        IOWR_SRAM_DATA(VGA_BASE, 0, bossXCoordinate);
        IOWR_SRAM_DATA(VGA_BASE, 15, bossYCoordinate);
    }
}

// close mouth
if(gameTime - openMouthTime > 0){
    //openMouthTime = 10000;
    IOWR_SRAM_DATA(VGA_BASE, 31, 0);
}

//bullet engaging
if(bulletFlag == 1){
    bulletXCoordinate = bulletXCoordinate + bulletXSpeed;
    if(bulletXCoordinate > xHighBound + 10){
        bulletFlag = 0;
    }
    IOWR_SRAM_DATA(VGA_BASE, 1, bulletXCoordinate);
    IOWR_SRAM_DATA(VGA_BASE, 14, bulletYCoordinate);
}

//bullet count
switch(bulletNumber){
case 0 : {
    IOWR_SRAM_DATA(VGA_BASE,26,800);
    IOWR_SRAM_DATA(VGA_BASE,25,800);
    IOWR_SRAM_DATA(VGA_BASE,24,800);
    IOWR_SRAM_DATA(VGA_BASE,23,800);
    IOWR_SRAM_DATA(VGA_BASE,22,800);
```



```
}break;
case 1 : {
    IOWR_SRAM_DATA(VGA_BASE,26,430);
    IOWR_SRAM_DATA(VGA_BASE,25,800);
    IOWR_SRAM_DATA(VGA_BASE,24,800);
    IOWR_SRAM_DATA(VGA_BASE,23,800);
    IOWR_SRAM_DATA(VGA_BASE,22,800);
}break;
case 2 : {
    IOWR_SRAM_DATA(VGA_BASE,26,430);
    IOWR_SRAM_DATA(VGA_BASE,25,450);
    IOWR_SRAM_DATA(VGA_BASE,24,800);
    IOWR_SRAM_DATA(VGA_BASE,23,800);
    IOWR_SRAM_DATA(VGA_BASE,22,800);
}break;
case 3 : {
    IOWR_SRAM_DATA(VGA_BASE,26,430);
    IOWR_SRAM_DATA(VGA_BASE,25,450);
    IOWR_SRAM_DATA(VGA_BASE,24,470);
    IOWR_SRAM_DATA(VGA_BASE,23,800);
    IOWR_SRAM_DATA(VGA_BASE,22,800);
}break;
case 4 : {
    IOWR_SRAM_DATA(VGA_BASE,26,430);
    IOWR_SRAM_DATA(VGA_BASE,25,450);
    IOWR_SRAM_DATA(VGA_BASE,24,470);
    IOWR_SRAM_DATA(VGA_BASE,23,490);
    IOWR_SRAM_DATA(VGA_BASE,22,800);
}break;
case 5 : {
    IOWR_SRAM_DATA(VGA_BASE,26,430);
    IOWR_SRAM_DATA(VGA_BASE,25,450);
    IOWR_SRAM_DATA(VGA_BASE,24,470);
    IOWR_SRAM_DATA(VGA_BASE,23,490);
    IOWR_SRAM_DATA(VGA_BASE,22,510);
}break;
}

//BOX created
int randNumberSeed2 = rand()%1000;
int randNumber2 = randNumberSeed2%100;
if(randNumber2 > 97 && boxFlag == 0){
    //assign random position
    boxXCoordinate = 620;
```

```

boxYCoordinate = (randNumberSeed/3) + 10;

if( boxYCoordinate >= 100){
    boxFlag = 1;
    //make sure enemy don't overlap for hardware
    for(j=0; j< 3; j++){
        if(abs(IORD_SRAM_DATA(VGA_BASE, 12-j) - boxYCoordinate) <=
80 && abs(IORD_SRAM_DATA(VGA_BASE, 3+j) - boxXCoordinate <= 60)){
            boxFlag = 0;
        }
    }
    if(boxFlag == 1){
        //printf("an      box      emerge      at      %d      \n
_____ ",boxYCoordinate);
    }
}
}
//box engaging
if(boxFlag == 1){
    boxXCoordinate = boxXCoordinate - boxXSpeed;
    if(boxXCoordinate < 19){
        boxFlag = 0;
        IOWR_SRAM_DATA(VGA_BASE, 20 , 800);
        IOWR_SRAM_DATA(VGA_BASE,21, 800);
        //printf("a box passed \n");
    }else{
        IOWR_SRAM_DATA(VGA_BASE,20, boxXCoordinate);
        IOWR_SRAM_DATA(VGA_BASE,21, boxYCoordinate);
    }
}

//hit boss happens
if(bulletFlag == 1 && bossFlag == 1 && abs(bulletXCoordinate-bossXCoordinate)
<= 40 && bulletYCoordinate - bossYCoordinate <= 80 && bulletYCoordinate -
bossYCoordinate >= -25) {
    //assign hit position
    //printf("hit boss happen \n");
    bossLife = bossLife - 1;
    if(bossLife == 0){
        // boss died
        bossFlag = 0;
        IOWR_SRAM_DATA(VGA_BASE,30, 0);
        // provide firework

```

```

        IOWR_SRAM_DATA(VGA_BASE, 7 , bossXCoordinate);
        IOWR_SRAM_DATA(VGA_BASE, 8 , bossYCoordinate);
        fireworkTime = gameTime;
        score = score + 200;
    }
    bulletFlag = 0;
    IOWR_SRAM_DATA(VGA_BASE, 1, 800);
    IOWR_SRAM_DATA(VGA_BASE, 14, 800);
    IOWR_SRAM_DATA(VGA_BASE, 0, 800);
    IOWR_SRAM_DATA(VGA_BASE, 15, 800);
    score = score + 30;
    IOWR_16DIRECT (AUDIO_BASE, 0 , 3);
    IOWR_16DIRECT (AUDIO_BASE, 0 , 4);
}
//hit enemy happens
for(i=0; i<3; i++){
    if(bulletFlag == 1 && enemyFlag[i] == 1 &&
abs(bulletXCoordinate-enemyXCoordinate[i]) <= 40 && bulletYCoordinate - enemyYCoordinate[i]
<= 80 && bulletYCoordinate - enemyYCoordinate[i] >= -25) {
        //assign hit position
        //printf("hit enemy happen , there are now %d enemies \n",
enemyCount);

        enemyFlag[i] = 0;
        bulletFlag = 0;
        enemyCount--;
        IOWR_SRAM_DATA(VGA_BASE, 1, 800);
        IOWR_SRAM_DATA(VGA_BASE, 14, 800);

        IOWR_SRAM_DATA(VGA_BASE, 3+i , 800);
        IOWR_SRAM_DATA(VGA_BASE,12-i, 800);
        score = score + 20;
        // provide firework
        IOWR_SRAM_DATA(VGA_BASE, 7 , enemyXCoordinate[i]);
        IOWR_SRAM_DATA(VGA_BASE, 8 , enemyYCoordinate[i]);
        IOWR_16DIRECT (AUDIO_BASE, 0 , 3);
        IOWR_16DIRECT (AUDIO_BASE, 0 , 4);
        fireworkTime = gameTime;
    }
}
//hit box
if(bulletFlag == 1 && boxFlag== 1 && abs(bulletXCoordinate-boxXCoordinate) <=
40 && bulletYCoordinate - boxYCoordinate <= 80 && bulletYCoordinate - boxYCoordinate >= -25)
{
    //assign hit position

```

```

        //printf("hit box happen \n");
        boxFlag = 0;
        bulletFlag = 0;
        bulletNumber = 5;
        IOWR_SRAM_DATA(VGA_BASE, 1, 800);
        IOWR_SRAM_DATA(VGA_BASE, 14, 800);

        IOWR_SRAM_DATA(VGA_BASE, 20, 800);
        IOWR_SRAM_DATA(VGA_BASE, 21, 800);
    }

    // shutdown firework
    if(gameTime - fireworkTime > 0){
        IOWR_SRAM_DATA(VGA_BASE, 7, 800);
        IOWR_SRAM_DATA(VGA_BASE, 8, 800);
    }

    //collision boss happens
    if(deadFlag == 0 && bossFlag == 1 && bossXCoordinate - playerXCoordinate>0 &&
bossXCoordinate - playerXCoordinate <= 40 && abs(bossYCoordinate - playerYCoordinate) <=
60){

        //assign collision happens
        deadFlag = 1;
        life = life - 1;

        IOWR_16DIRECT (AUDIO_BASE, 0, 1);
        IOWR_16DIRECT (AUDIO_BASE, 0, 2);
        //printf("player is dead contacting boss, has life %d \n", life);
    }

    //collision enemy happens
    for(i=0; i < 3; i++){
        if(deadFlag == 0 && enemyFlag[i] == 1 && enemyXCoordinate[i] -
playerXCoordinate>0 && enemyXCoordinate[i] - playerXCoordinate <= 40 &&
abs(enemyYCoordinate[i] - playerYCoordinate) <= 60){
            //assign collision happens
            deadFlag = 1;
            enemyFlag[i] = 0;
            enemyCount--;
            life = life - 1;

            IOWR_16DIRECT (AUDIO_BASE, 0, 1);
            IOWR_16DIRECT (AUDIO_BASE, 0, 2);
            //printf("player is dead contacting enemy, has life %d \n", life);
        }
    }
}

```

```
        IOWR_SRAM_DATA(VGA_BASE, 3 + i, 800);
        IOWR_SRAM_DATA(VGA_BASE, 12 - i, 800);
    }
}
//collision box happens
if(boxFlag == 1 && boxXCoordinate - playerXCoordinate>0 && boxXCoordinate -
playerXCoordinate <= 40 && abs(boxYCoordinate - playerYCoordinate) <= 60){
    //assign collision happens
    boxFlag = 0;
    bulletNumber = bulletNumber + 3;
    if(bulletNumber > 5){
        bulletNumber = 5;
    }
    IOWR_SRAM_DATA(VGA_BASE, 20 , 800);
    IOWR_SRAM_DATA(VGA_BASE, 21, 800);
    //printf("player get bullet, has bullet %d \n", bulletNumber);
}

if(life == 3){
    IOWR_SRAM_DATA(VGA_BASE,29,270);
    IOWR_SRAM_DATA(VGA_BASE,28,300);
    IOWR_SRAM_DATA(VGA_BASE,27,330);
}
if(life == 2){
    IOWR_SRAM_DATA(VGA_BASE,27,800);
}
if(life == 1){
    IOWR_SRAM_DATA(VGA_BASE,28,800);
}

//game over happen
if(life == 0){
    int loop = 0;
    for(loop = 0; loop < 100000; loop++){
        //create game over
        IOWR_SRAM_DATA(VGA_BASE,29,800);

        IOWR_SRAM_DATA(VGA_BASE,0,800);
        IOWR_SRAM_DATA(VGA_BASE,1,800);
        IOWR_SRAM_DATA(VGA_BASE,2,800);
        IOWR_SRAM_DATA(VGA_BASE,3,800);
        IOWR_SRAM_DATA(VGA_BASE,4,800);
        IOWR_SRAM_DATA(VGA_BASE,5,800);
```

```
IOWR_SRAM_DATA(VGA_BASE,7,800);
IOWR_SRAM_DATA(VGA_BASE,20, 800);
if(finalScore == 0){
    finalScore = score;
}
if(finalScore > 200){
    IOWR_SRAM_DATA(VGA_BASE, 19, 2);
}else if(finalScore <= 200 && finalScore > 100){
    IOWR_SRAM_DATA(VGA_BASE, 19, 3);
}else if(finalScore <=100 && finalScore >= 0){
    IOWR_SRAM_DATA(VGA_BASE, 19, 4);
}
}

IOWR_SRAM_DATA(VGA_BASE,19,1); // init begin display

//init display all out the screen
IOWR_SRAM_DATA(VGA_BASE,0,800);
IOWR_SRAM_DATA(VGA_BASE,1,800);
IOWR_SRAM_DATA(VGA_BASE,2,800);
IOWR_SRAM_DATA(VGA_BASE,3,800);
IOWR_SRAM_DATA(VGA_BASE,4,800);
IOWR_SRAM_DATA(VGA_BASE,5,800);
IOWR_SRAM_DATA(VGA_BASE,7,800);
IOWR_SRAM_DATA(VGA_BASE,20, 800);
IOWR_SRAM_DATA(VGA_BASE,9,0);
IOWR_SRAM_DATA(VGA_BASE,16,0);
IOWR_SRAM_DATA(VGA_BASE,17,0);
IOWR_SRAM_DATA(VGA_BASE,18,0);
IOWR_SRAM_DATA(LEDS_BASE, 0, 0);
IOWR_SRAM_DATA(LEDS_BASE, 1, 0);
IOWR_SRAM_DATA(LEDS_BASE, 2, 0);
IOWR_SRAM_DATA(LEDS_BASE, 3, 0);
IOWR_SRAM_DATA(VGA_BASE,26,800);
    IOWR_SRAM_DATA(VGA_BASE,25,800);
    IOWR_SRAM_DATA(VGA_BASE,24,800);
    IOWR_SRAM_DATA(VGA_BASE,23,800);
    IOWR_SRAM_DATA(VGA_BASE,22,800);

while(IORD_SRAM_DATA(VGA_BASE, 19) != 0){
```

```
int beginSound = IORD_16DIRECT(AUDIOSLAVE_BASE,0);
if( beginSound < 4500 || beginSound >61035 || (beginSound>32000 &&
beginSound< 33000)){
    // threshold move up 1000
    startFlag = 0;
}else{
    startFlag++;
    if(startFlag > 25){
        startFlag = 0;
        IOWR_SRAM_DATA(VGA_BASE,19,0);
    }
}
}
```

```
playerXCoordinate = 40;    // init positions
playerYCoordinate = 360;
bossXCoordinate = 550;
bossYCoordinate = 400;
bulletXCoordinate = 600;
bulletYCoordinate = 480;
boxXCoordinate = 800;
boxYCoordinate = 800;
```

```
playerYSpeed = 1; //init speeds
enemyXSpeed = 1;
bossXSpeed = 0;
bossYSpeed = 0;
bulletXSpeed = 4;
boxXSpeed = 2;
```

```
deadFlag = 0; //int flags
bossFlag = 0;
bulletFlag = 0;
boxFlag = 0;
life = 3; //init lifes
bulletNumber = 5;
```

```
int i = 0; //init for enemyflags
int j = 0;
for(i = 0; i < 10; i++){
    enemyFlag[i] = 0;
    enemyXCoordinate[i] = 800;
    enemyYCoordinate[i] = 800;
```

```
    }
    enemyCount = 0;

    counterTime = 500;    //init counters
    counterDrop = 500;
    counterFly = 500;
    counterNormal = 500;

    srand(time(NULL));    //init rand seed

    IOWR_SRAM_DATA(VGA_BASE,31, 0); // init player and boss initial faces
    IOWR_SRAM_DATA(VGA_BASE,30, 0);

    openMouthTime = 0;    //init animation time
    fireworkTime = 0;
    gameTime = 0;
        openMouthTime = 0;
        bossYSpeed = 0;
        bossXSpeed = 0;
        finalScore = 0;
        score = 0;
    }

    //finish game
    if(gameTime > 90){
        // player survive
        gameTime = 0;
        openMouthTime = 0;
        bossYSpeed = 0;
        bossXSpeed = 0;
        enemyXSpeed = enemyXSpeed * 2;
        bossYSpeed = bossYSpeed * 2;
        bossLife = 1000;
        //printf("time out . next round speed * 2 \n");
        //printf("score is %d", score);
    }
}
}
```

H_control.vhd, for background display project

--Build it with VGA top in SOPC

library ieee;

use ieee.std_logic_1164.all;

use ieee.numeric_std.all;

entity H_control is

port(

 clk : in std_logic;
 Hcount : in unsigned(9 downto 0);
 Pattern_H : in integer;
 locate : in integer;
 Hcounter : buffer integer;
 flag_h : out std_logic
);

end entity H_control;

architecture rtl of H_control is

 constant HSYNC : integer := 96;

 constant HBACK_PORCH : integer := 48;

begin

 process(clk)

 begin

 if rising_edge(clk) then

-- if locate > 20 then

 if Hcount < HSYNC + HBACK_PORCH - 1 + locate then

 flag_h <= '0';

 elsif Hcount = HSYNC + HBACK_PORCH - 1 + locate then

 flag_h <= '1';

 Hcounter <= 0;

 elsif Hcount > HSYNC + HBACK_PORCH - 1 + locate and Hcount < HSYNC +
HBACK_PORCH - 1 + locate + Pattern_H then

 Hcounter <= Hcounter +1;

 elsif Hcount >= HSYNC + HBACK_PORCH - 1 + locate + Pattern_H then

 Hcounter <= 0;

 flag_h <= '0';

 end if;

-- else

-- flag_h <='0';

-- end if;

 end if;

```
    end process;  
end rtl;
```