DC Motor Controller

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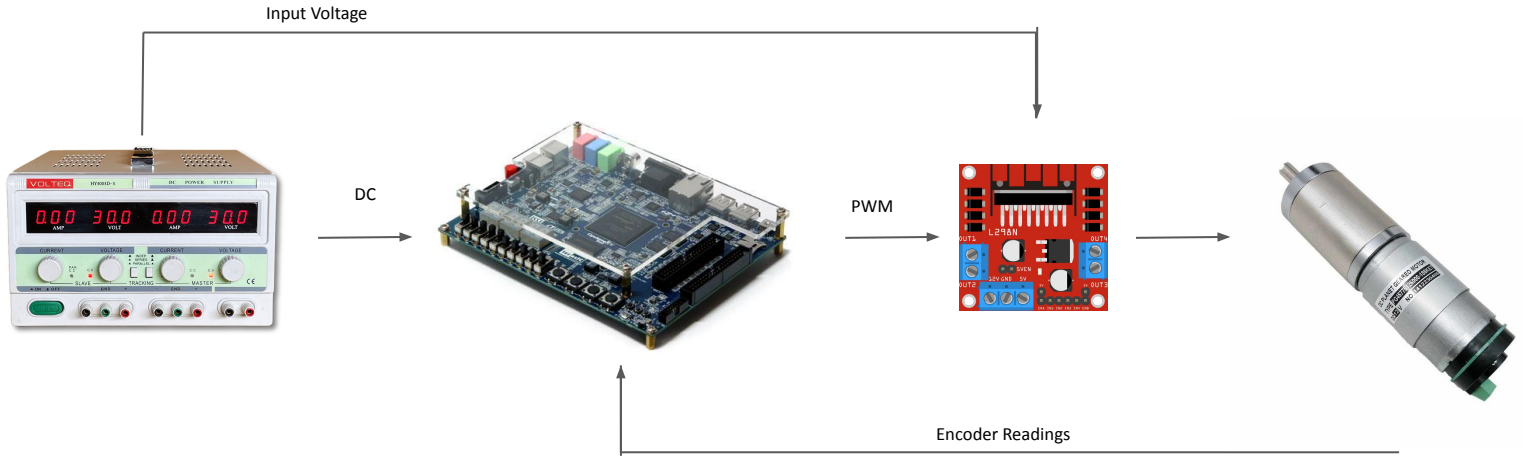
Final Project Proposal
EECS E6692 Spring ‘22 Embedded Systems
Columbia University
Prof. Stephen Edwards

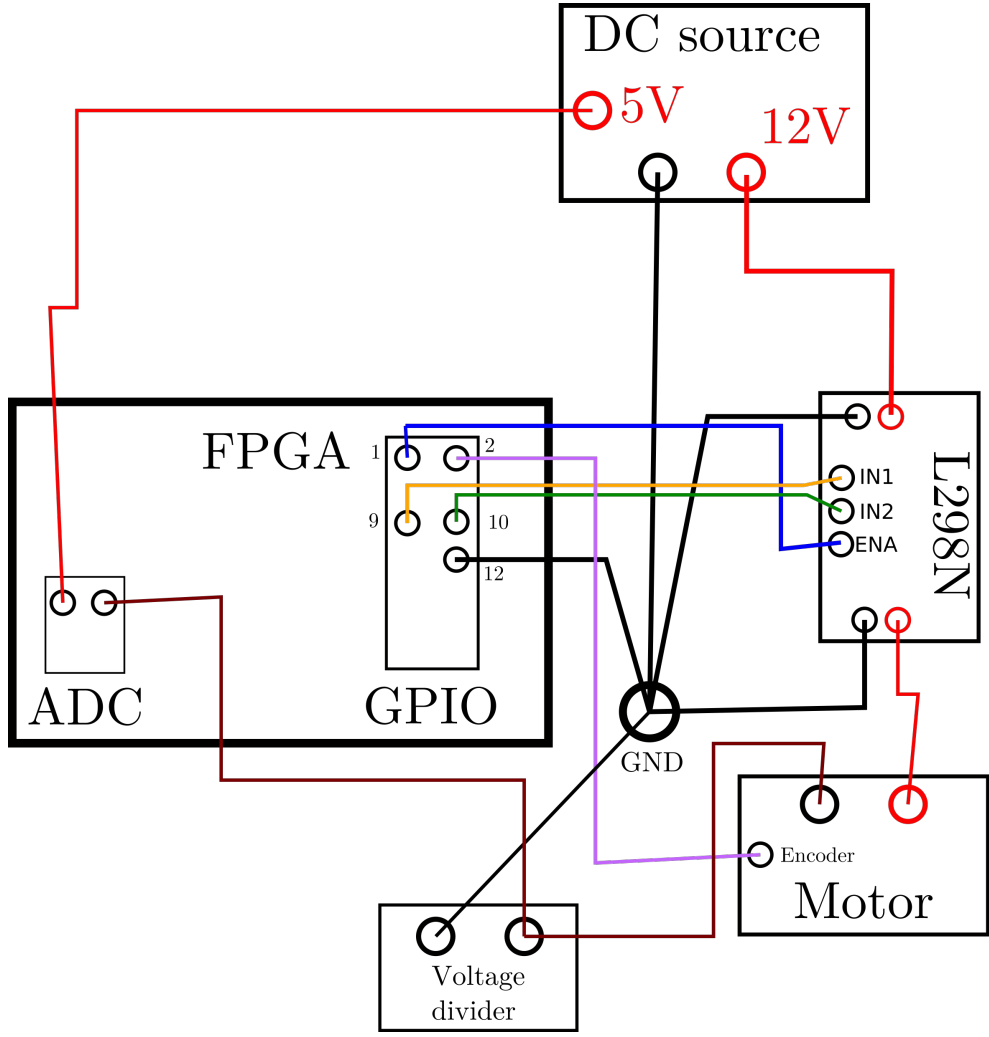
Why Motor Control on the FPGA:

- There are many additional advantages when these are designed on FPGAs, such as the ability to use custom pulse-width modulation (PWM), easier component integration, fewer components, higher control-loop bandwidth, and higher reliability.
- The purpose of our project was to design an actual DC motor controller that takes full advantage of the FPGA's capabilities and can be implemented in actual industrial level applications, where the system and control laws have been thoroughly studied before implementation.
- We have attached a brief overview of our project components and their connections below



Global system

- GPIO:
  - receive data from the encoder;
  - Control the H-bridge via PWM;
- ADC:
  - Speed control through the DC source (potentiometer)
  - Current feedback thanks a voltage divider
- L298N:
  - Embeds an H-Bridge
- Besides:
  - User interface with the switches on the FPGA



ADC LTC2308

- The embedded ADC converter—LTC2308 on the DE1 SoC board is a low noise, 500Ksps, 8-channel, 12-bit ADC module with an SPI compatible serial interface.

- We have written our code according to the timing diagram, as shown in the documentation of the LTC2308.

- We opt to make use of the CLK input clock signal for our SCK, which controls the SDI and SDO at negative edge activations, and have written the rest of our code, including the configuration bits of the SDI and the output bits from the SDO using this logic. Further details are in the report

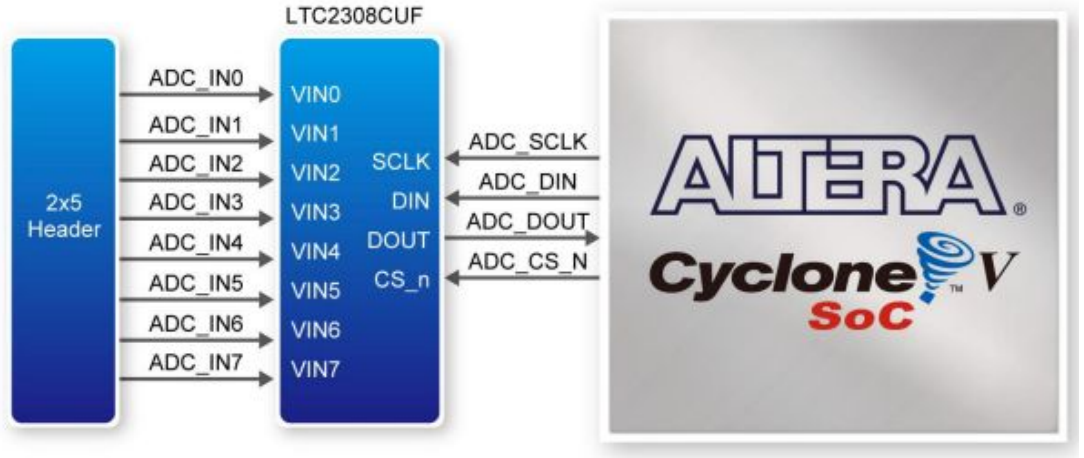
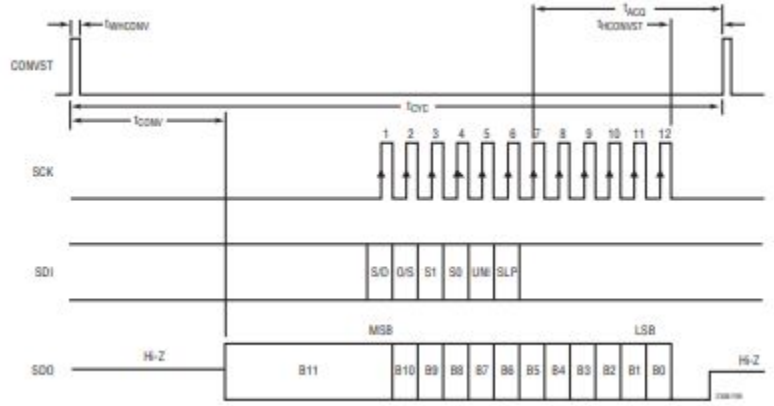
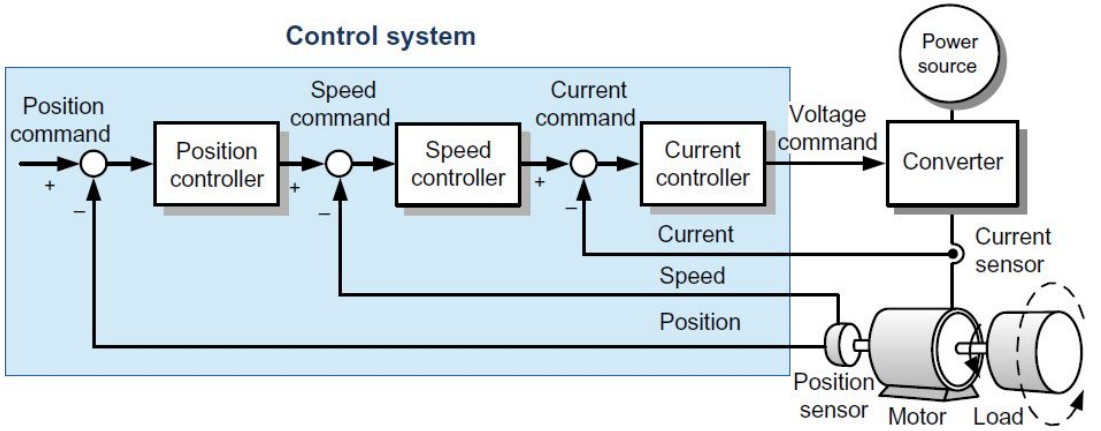


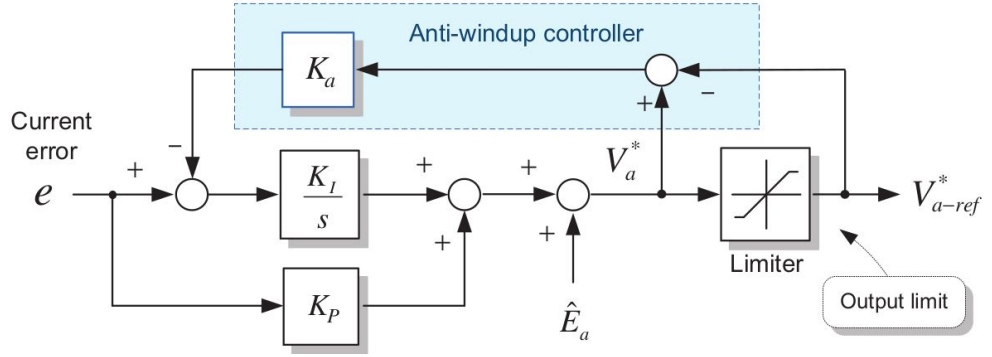
Figure 3-31 Connections between the FPGA, 2x5 header, and the A/D converter



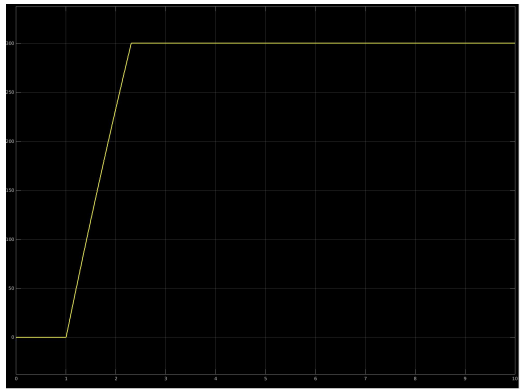
Controller

- Cascade control framework:
  - Proportional-integral current controller (nested);
  - Proportional-integral speed controller;
- Discretization of the controller
- Implementation in C
  - Recursive sequences

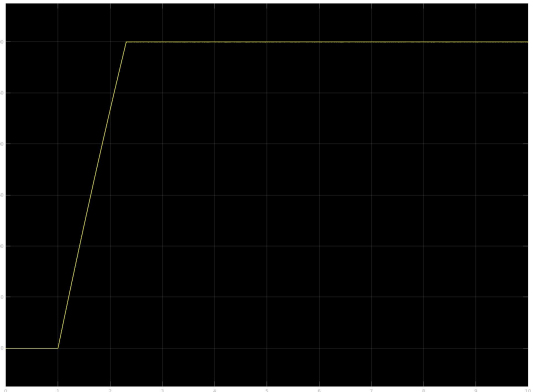




Current controller



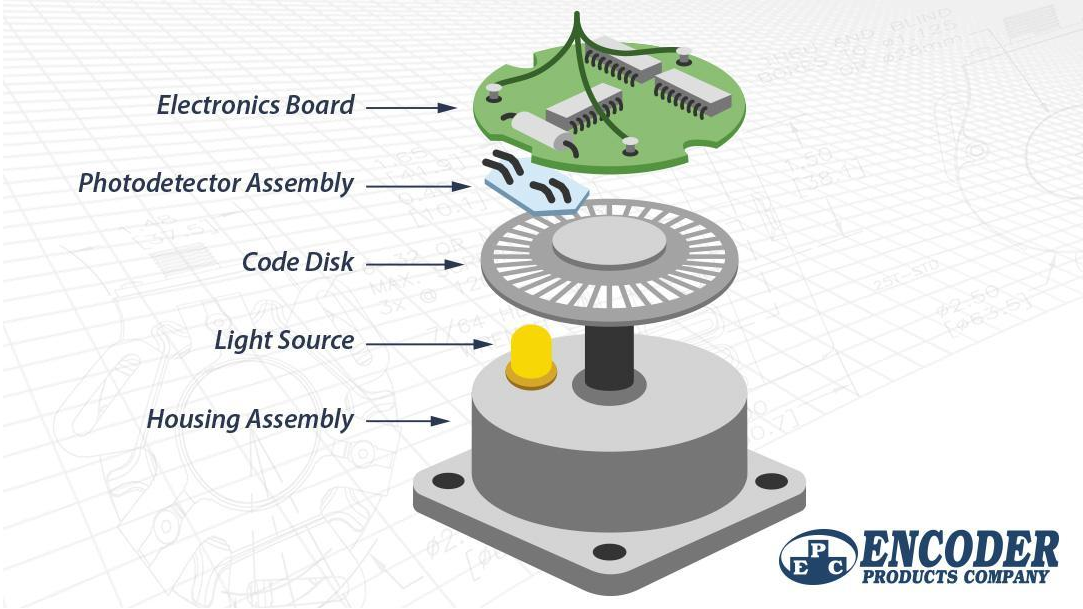
Continuous speed output



Discretized speed output

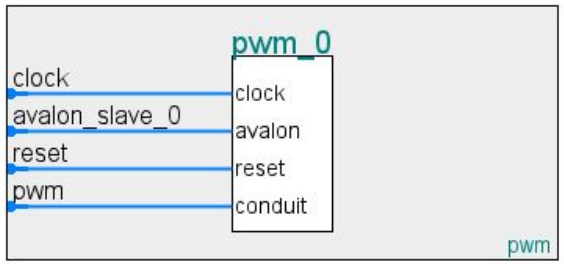
Encoder

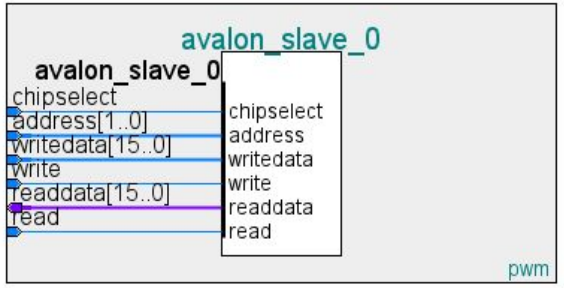
- 7 pulses per turn
- Processed by a GPIO pin of the FPGA
- Data sent to software at a 100 Hz
- Minimum speed that can be measured: 1000 RPM

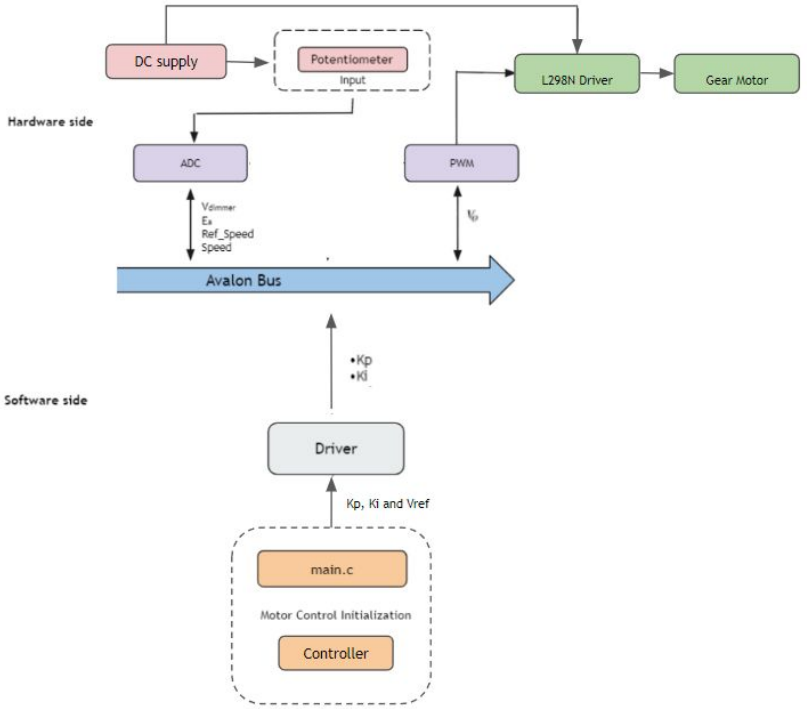


HW-SW interface

- Module pwm
  - Embeds the pwm function (receives data and write duty cycle)
  - Processes the data from the encoder (send them to the software)
- One driver for this peripheral
  - Ready to communicate for the ADC data too



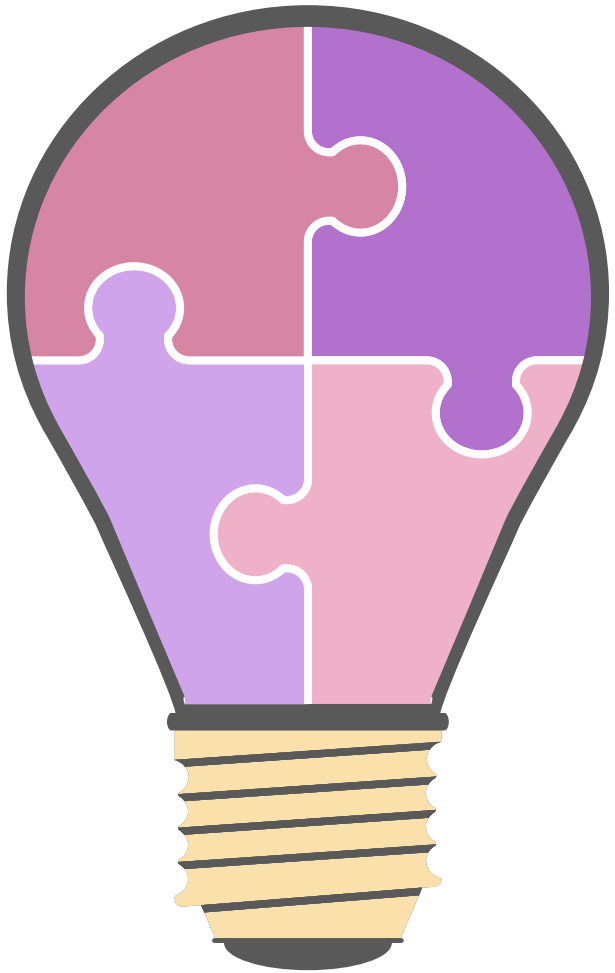




Conclusion and Future Work

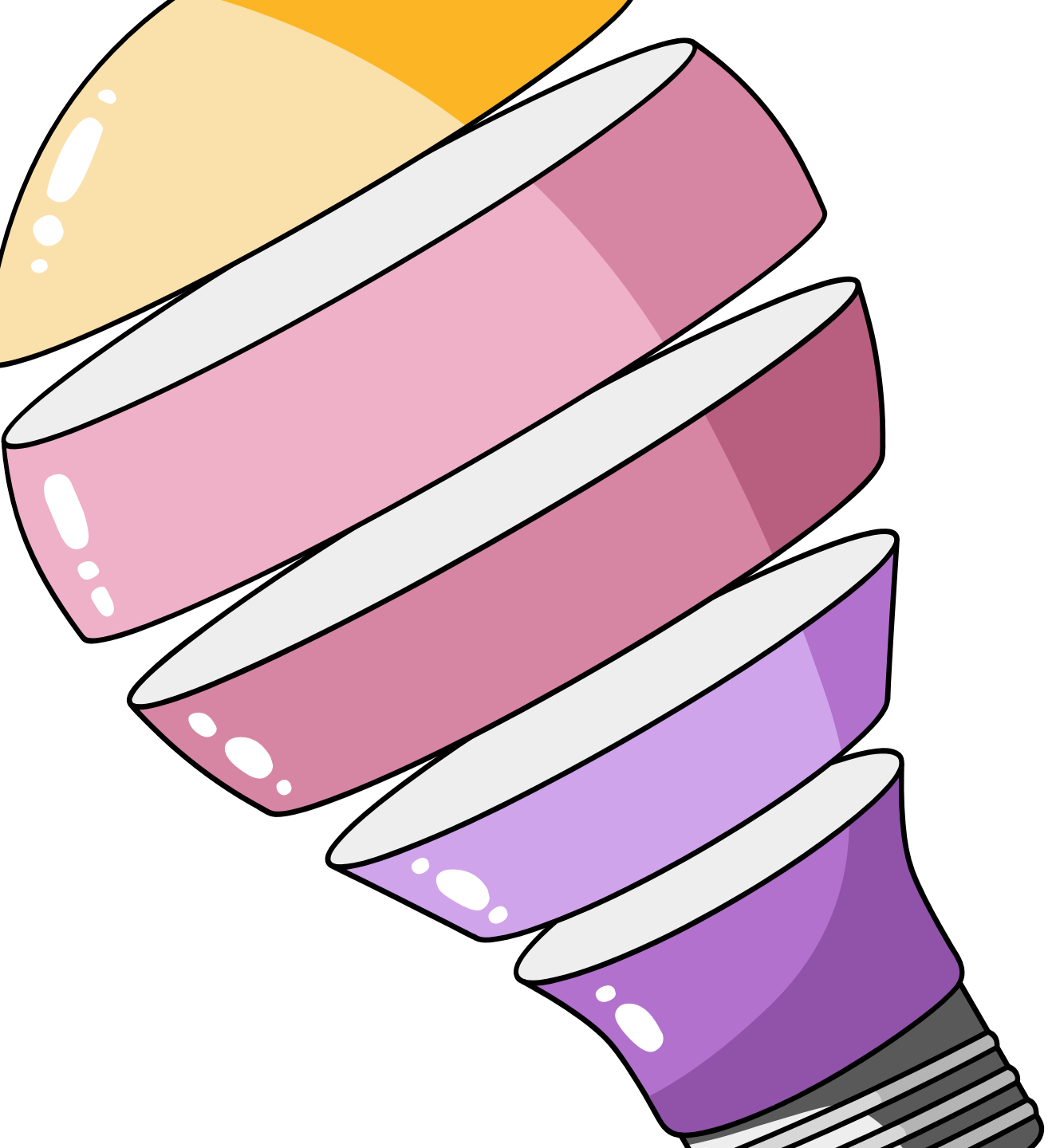
Conclusion..

In this report, we have presented a project that has aimed to design and implement an industrial DC motor controller by taking in input commands that can be set by the user during runtime.



Future work..

While not perfect, we believe that this FPGA based motor controller project has a lot of potential as it can be generalized to many different motor ratings. With a little bit of polishing, this work can be extended to a plethora of applications including robotic arm control, electric vehicles, and so on..



Thank You