Separate Compilation for Synchronous Modules

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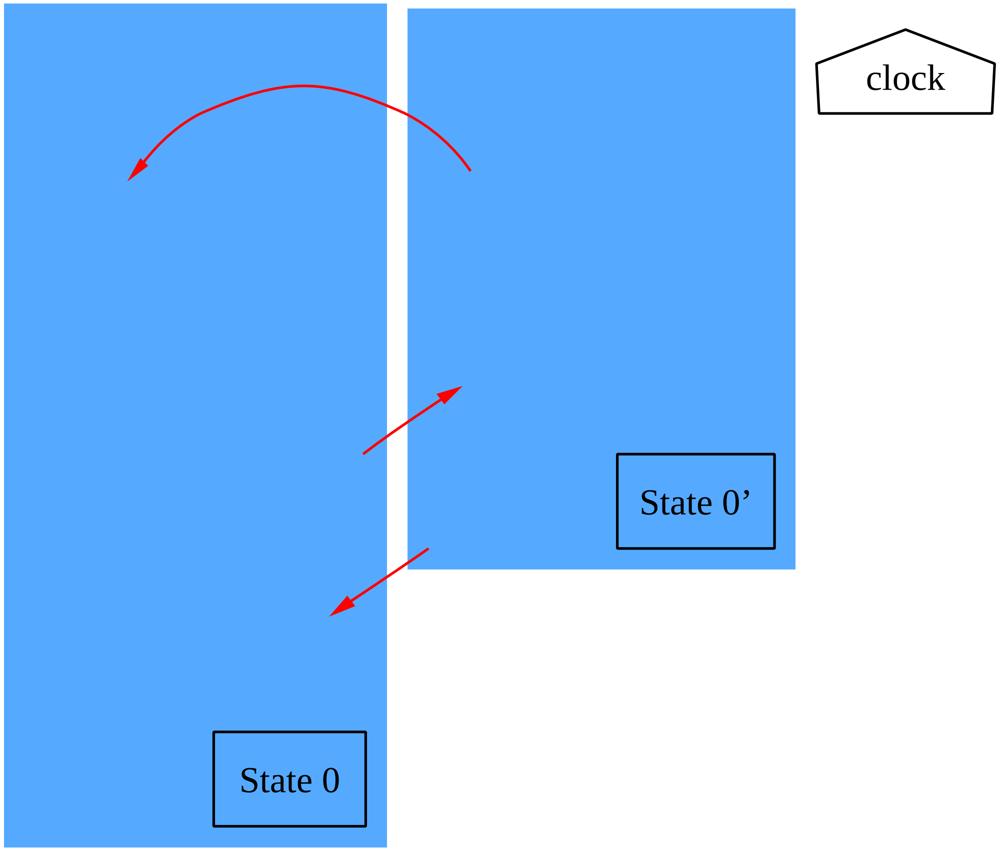
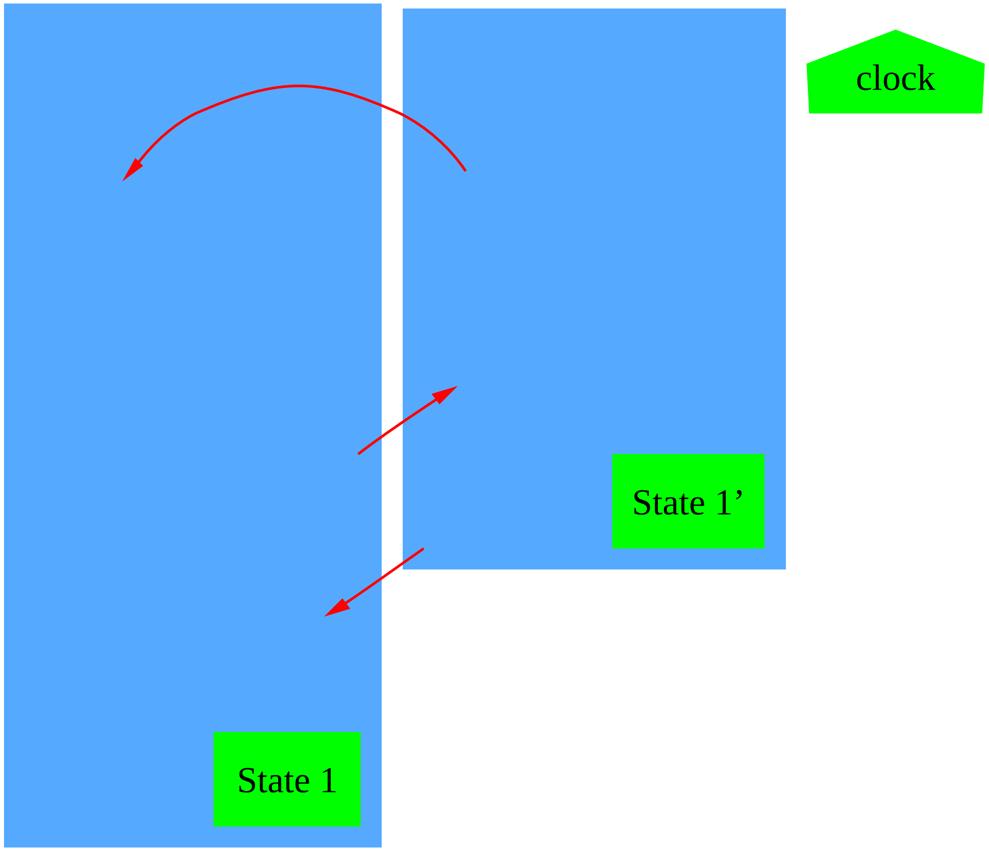
Motivation

- Synchronous model for hardware design



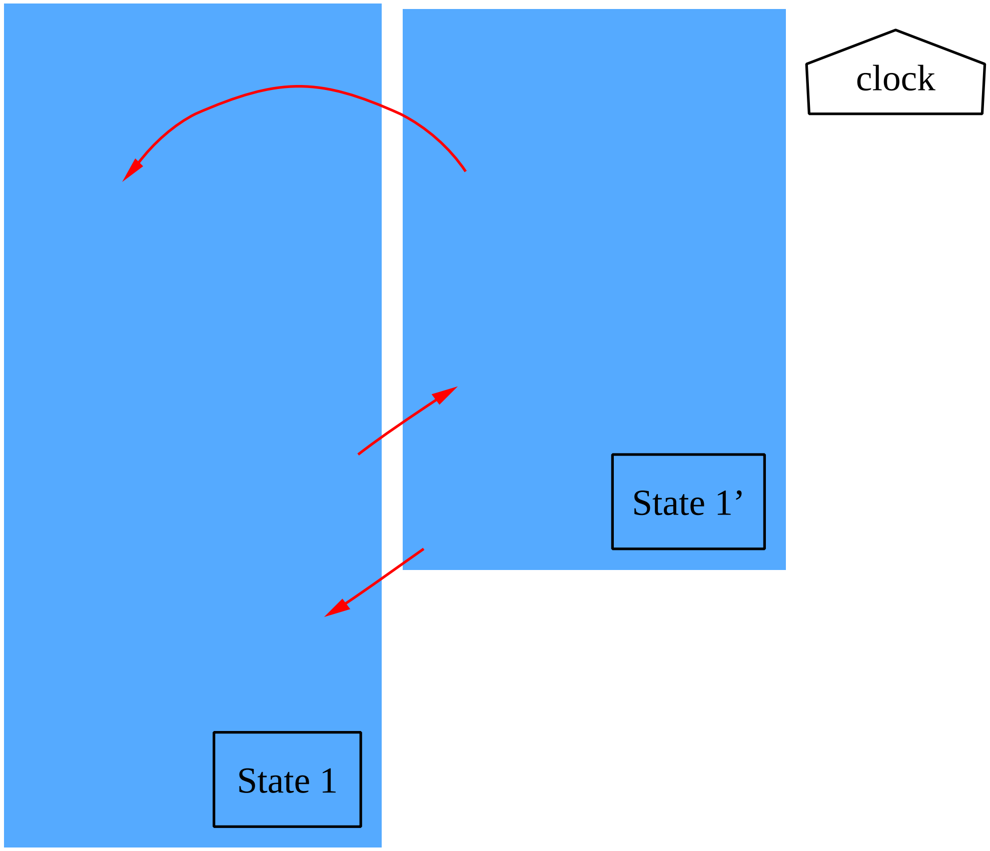
Motivation

- State changed when clock is on.



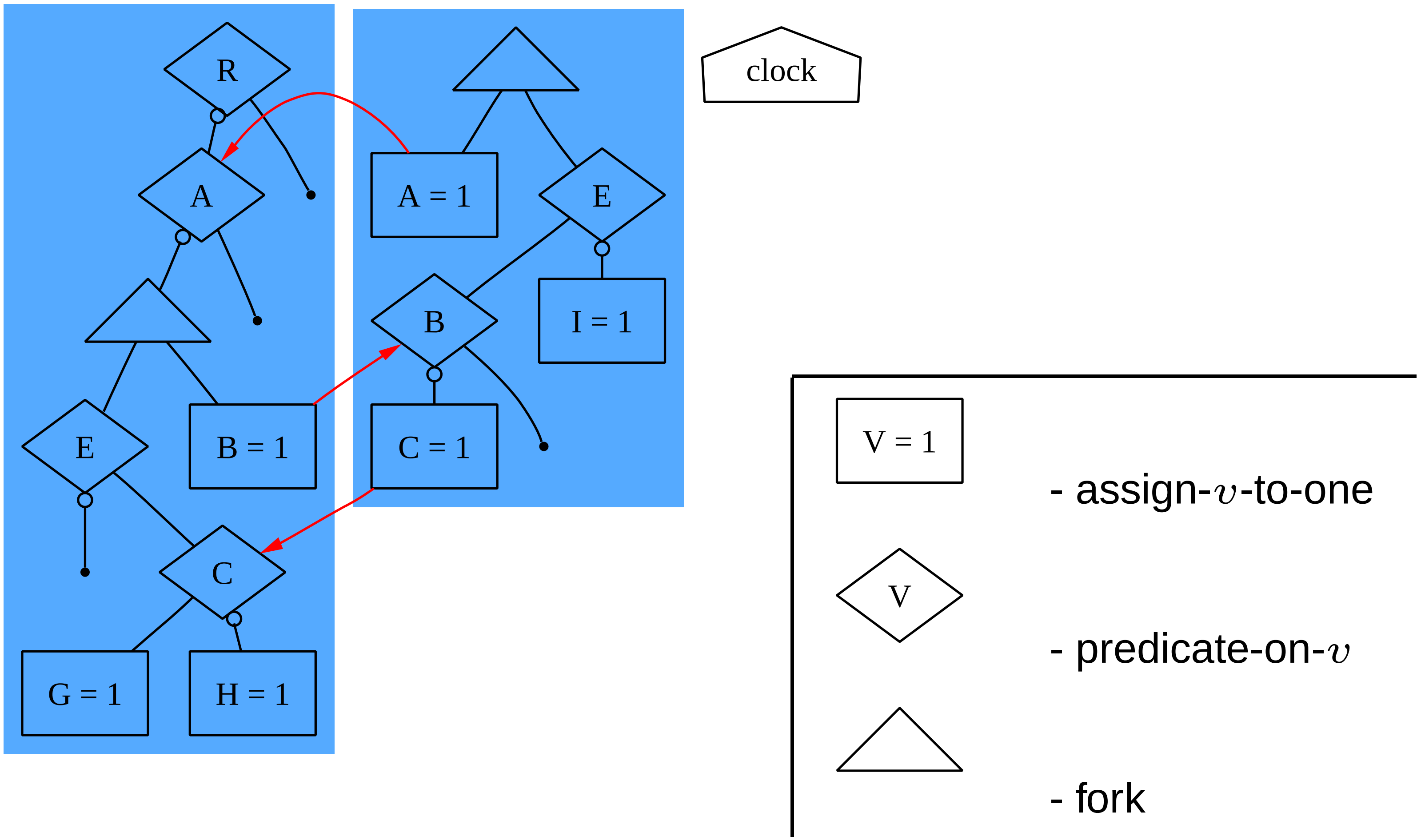
Motivation

- State remains same when clock is off.



Motivation

- An instance of the system inside a clock cycle



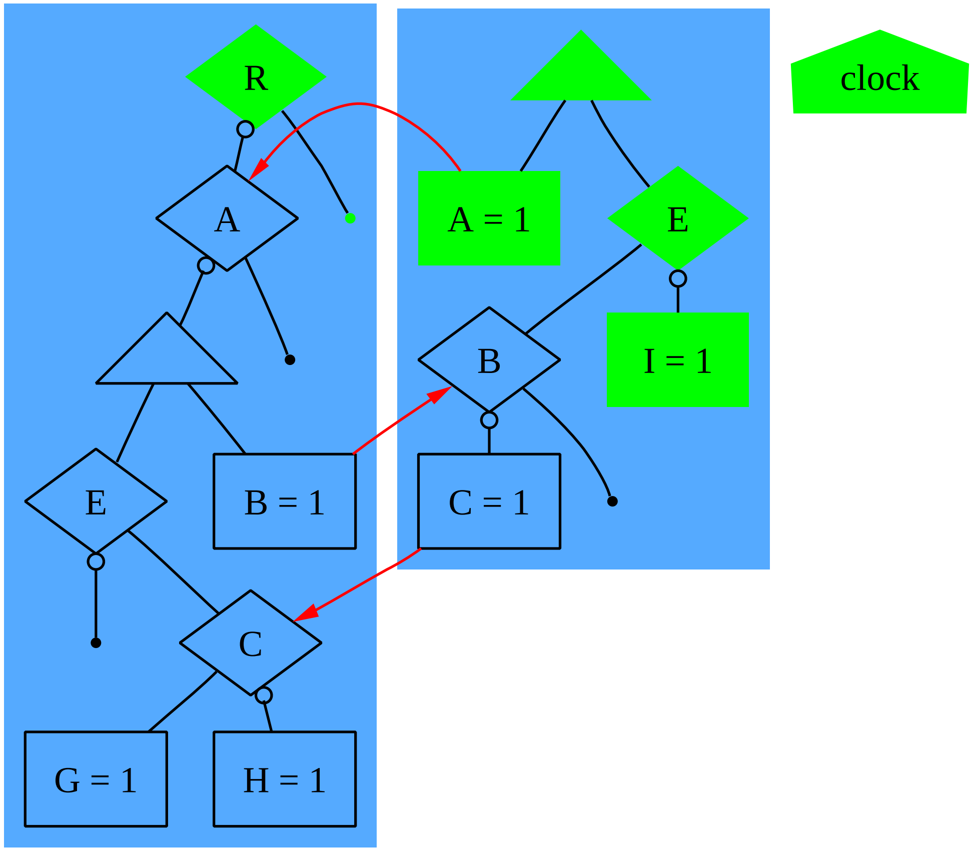
- assign-υ-to-one

- predicate-on-υ

- fork

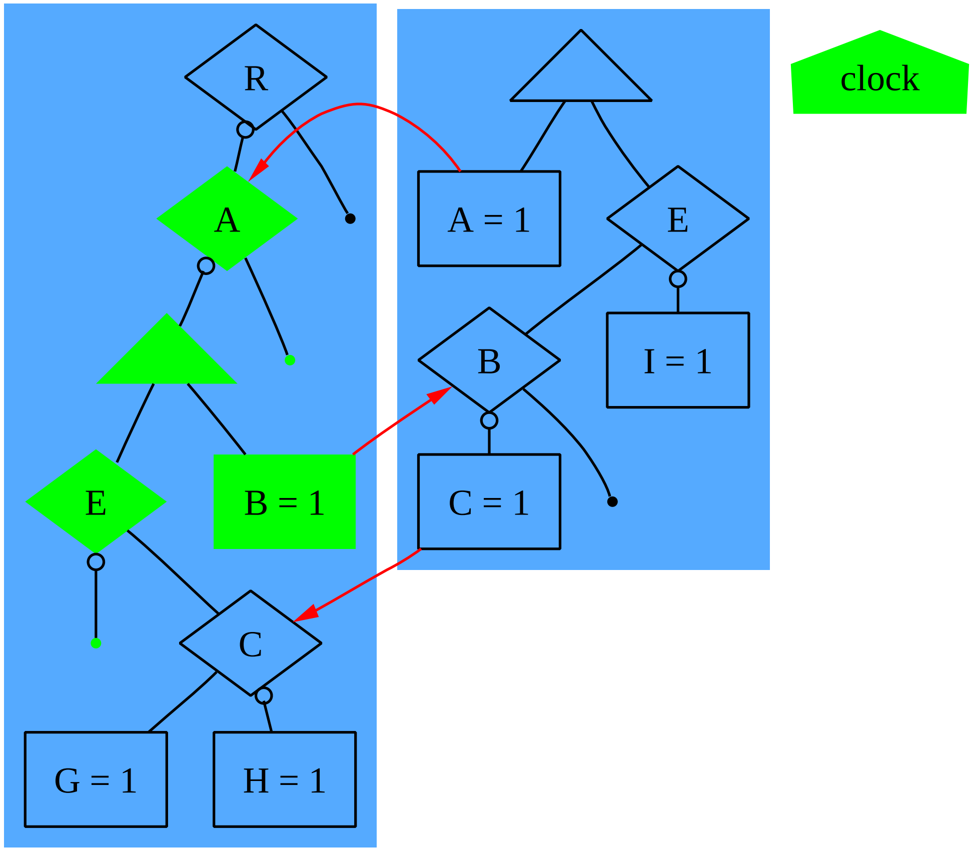
Motivation

- Simulation rule: assignment before predicate



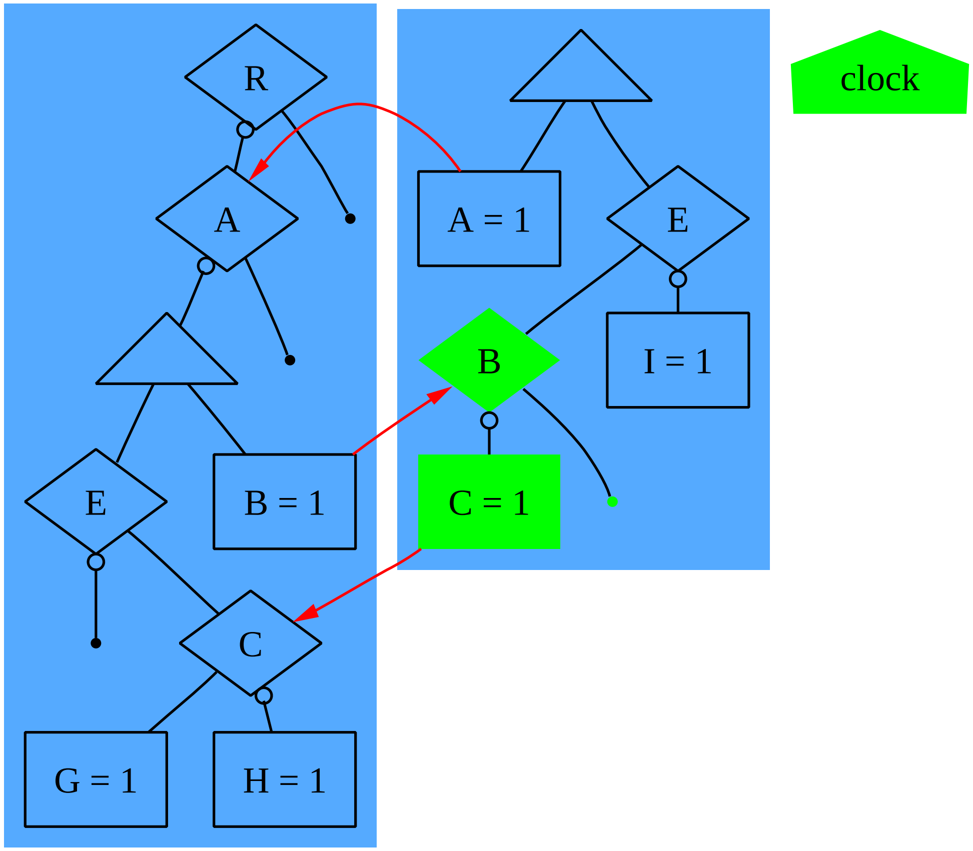
Motivation

- Simulate an instance of the whole system



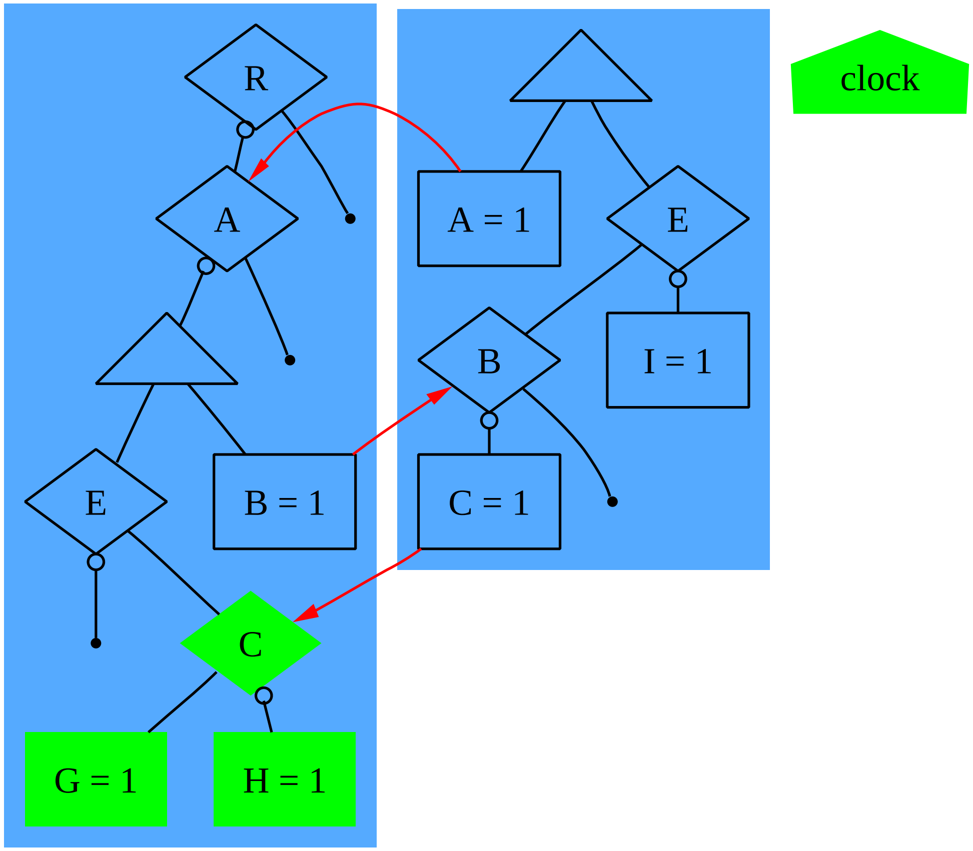
Motivation

- Simulate an instance of the whole system



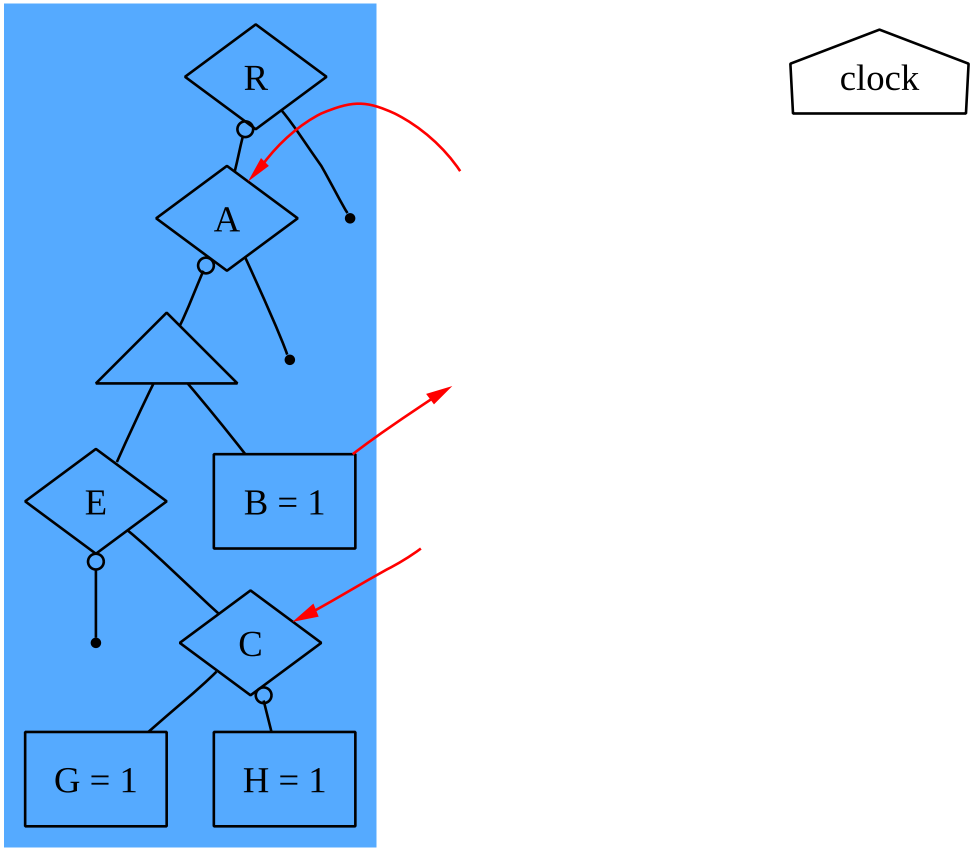
Motivation

- Simulate an instance of the whole system



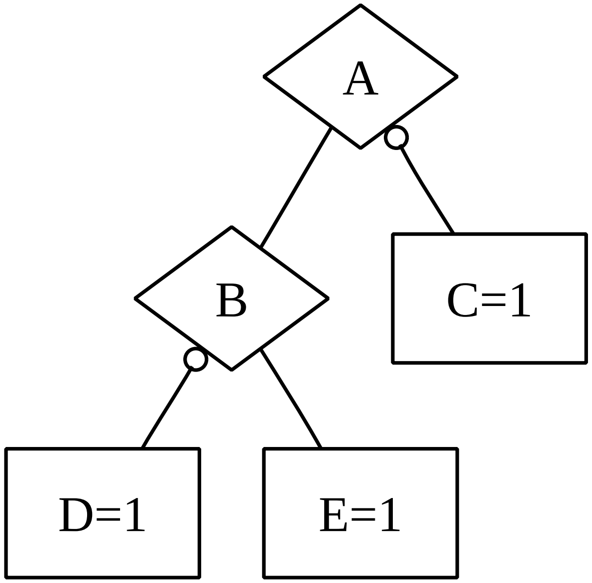
Motivation

- Separate compilation/simulation: is B monotonic?

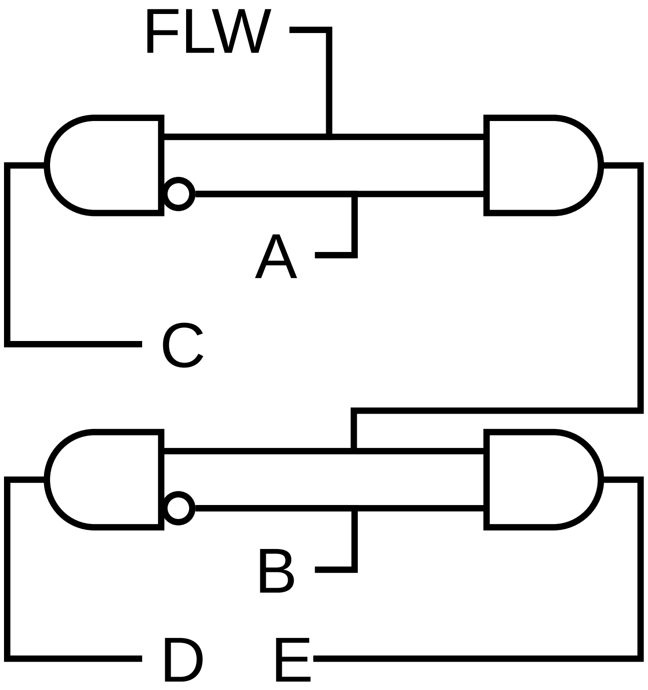


Previous Work

- Verilog/VHDL: simulate at circuit level
- 3-value logic computation



2-Valued CFG

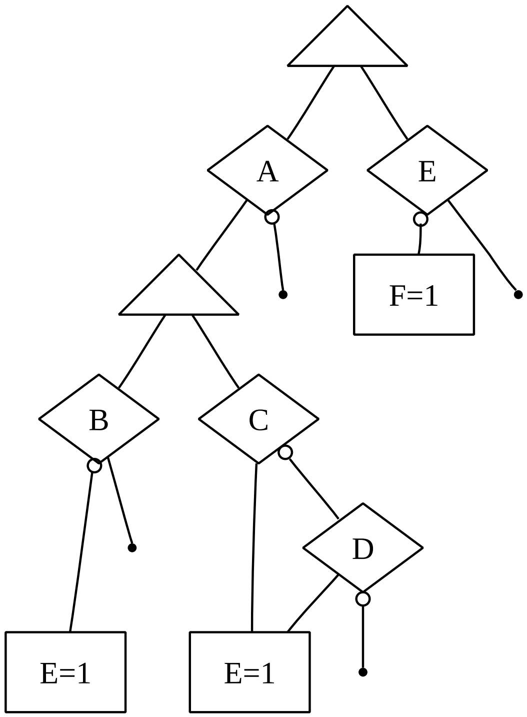


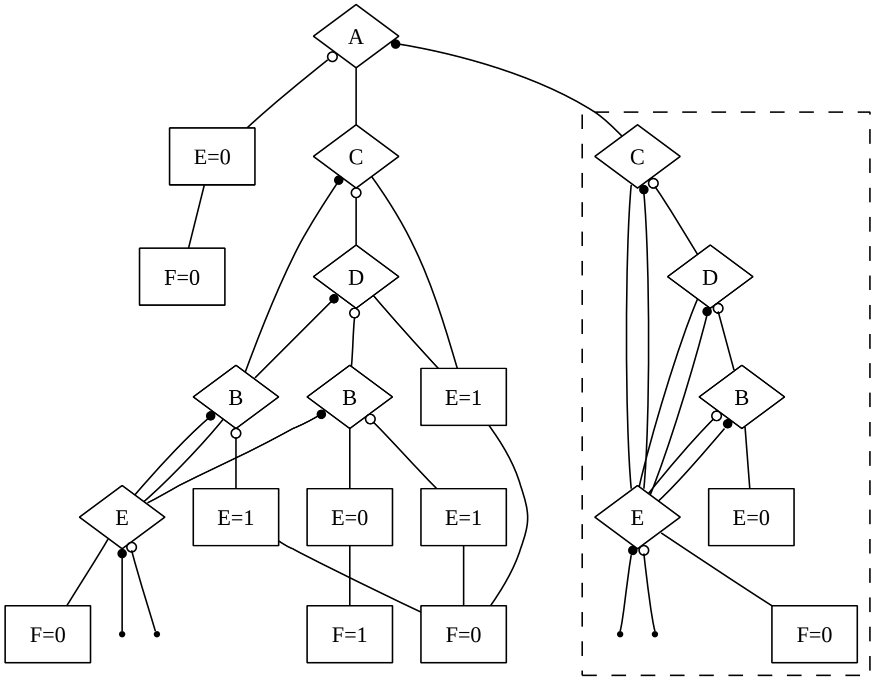
3-Valued Domain Simulation

Our Work

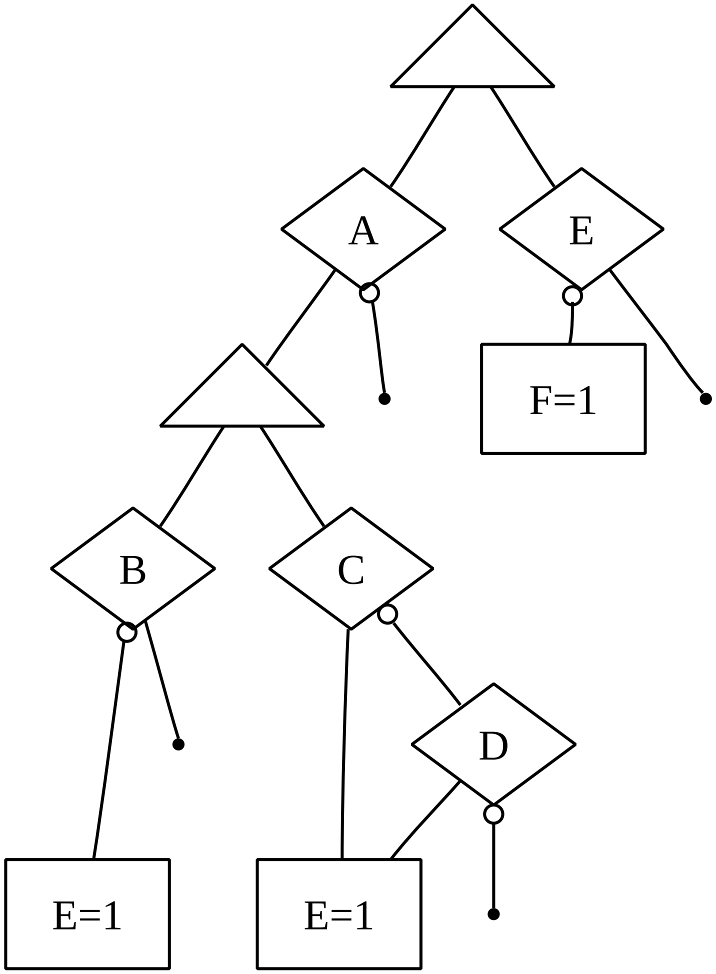
- Algorithm
  - Build constructive graph by partial evaluation;
  - Exponential size in theory;
  - Minimized size by sharing nodes;
  - Neither BDD nor simple decision diagram;
  - Sequentialize program as side-effect.
- Implementation:
  - CEC - Columbia Esterel Compiler
  - Build constructive GRaph Code (GRC)

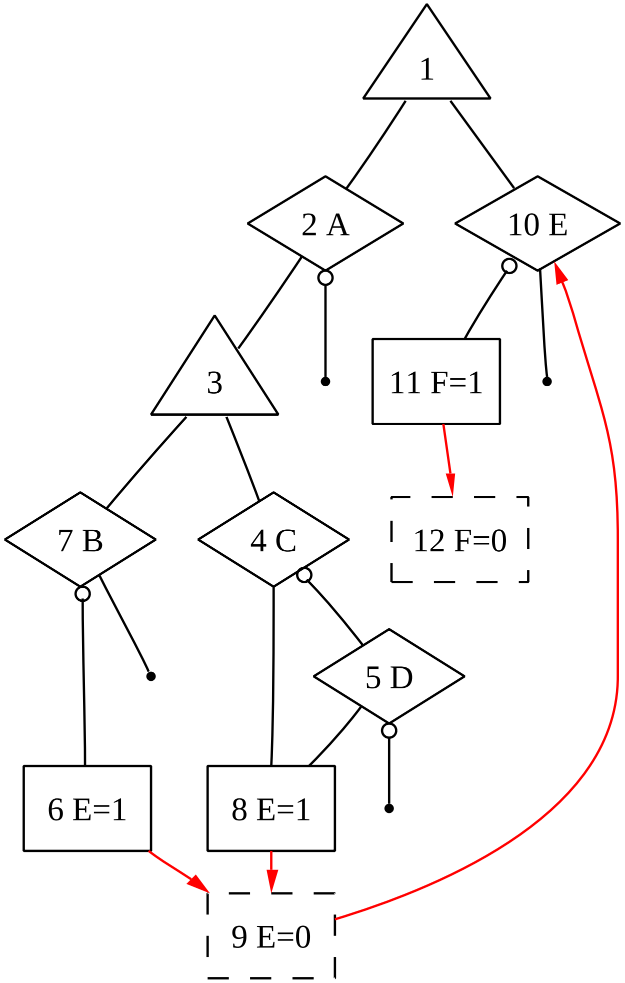
Construction Example: 2-valued to 3-valued





Example - Step 1: Add Assign-v-to-0





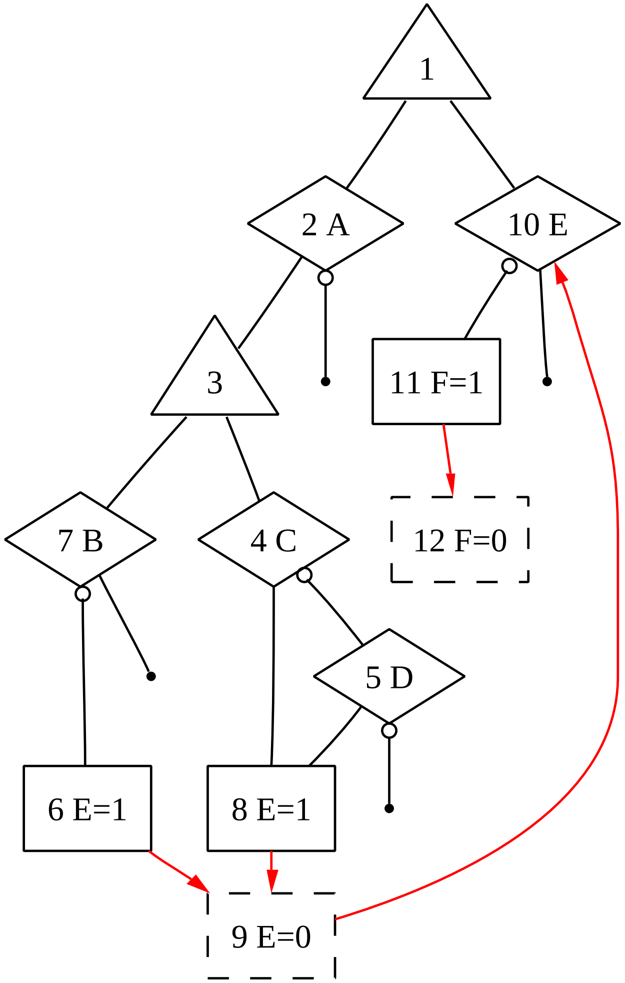
Example - Step 2: Ctrl State Init

A	B	C	D	E	F
?	?	?	?	?	?

Table 1: variable state

1	2	3	4	5	...
1					

Table 2: node state



Example - Step 3: Ctrl Propagation

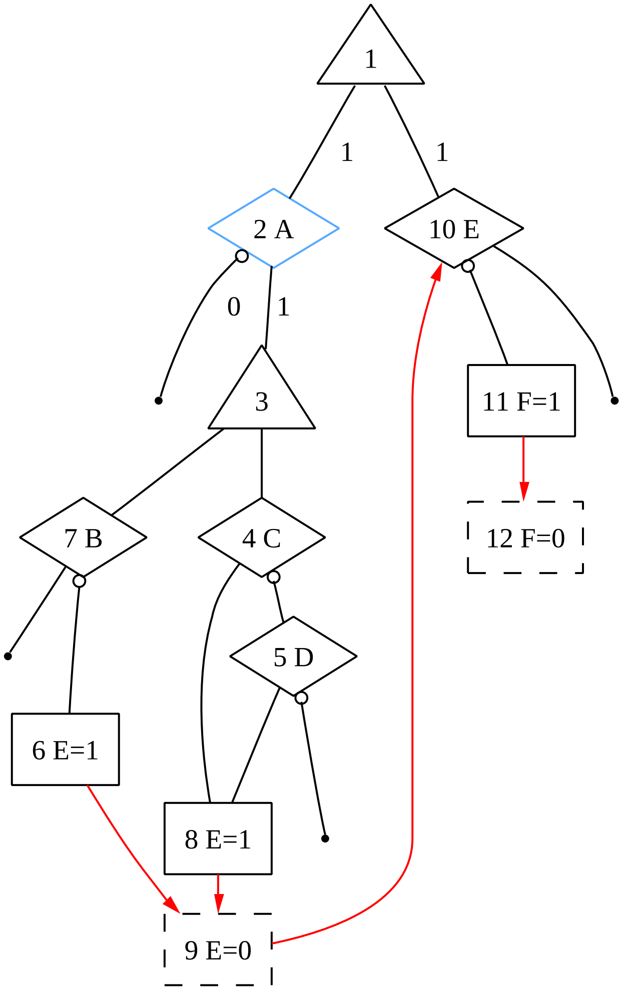
A = 1, Visiting Node 2:

A	B	C	D	E	F
1	?	?	?	?	?

Table 3: variable state

1	2	3	4	...	12
1	1				

Table 4: node state



Example - Step 3: Ctrl Propagation

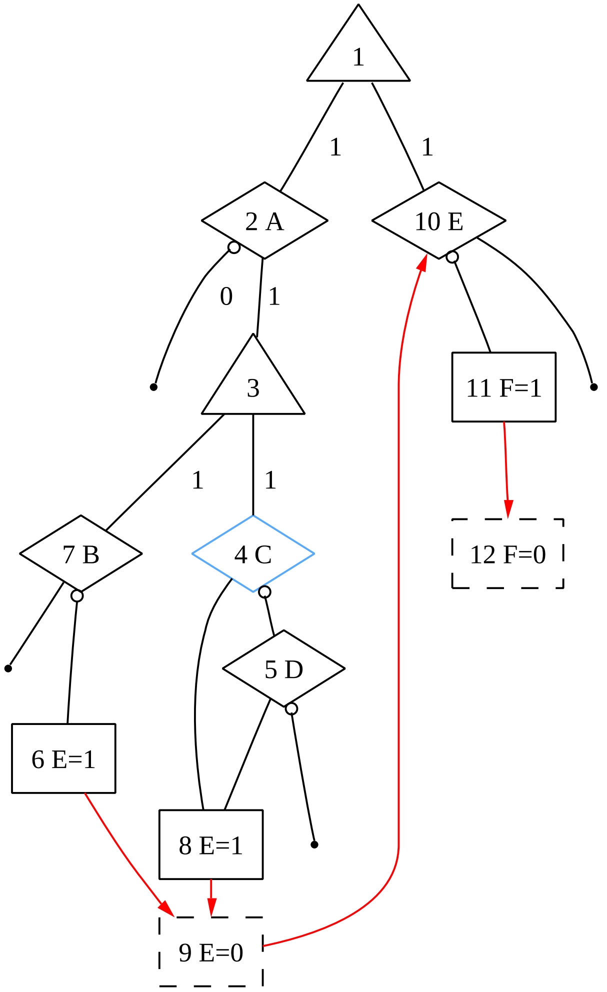
A = 1, Visiting Node 4:

A	B	C	D	E	F
X	?	?	?	?	?

Table 5: variable state

1	2	3	4	...	12
1	1	1	1		

Table 6: node state



Example - Step 3: Ctrl Propagation

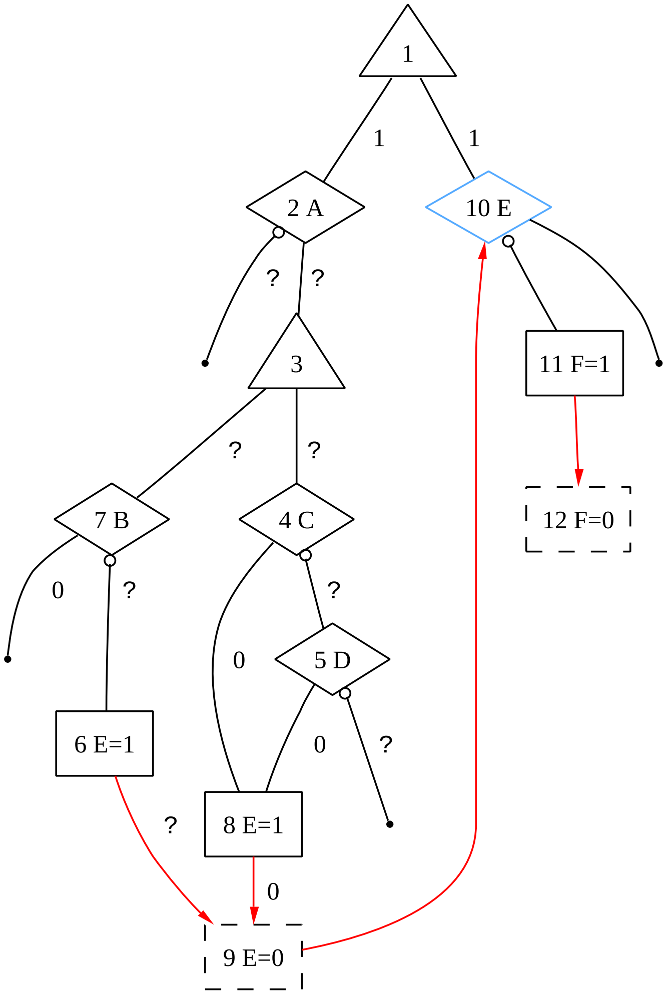
A = ?, B = C = D = 0, Node 10:

A	B	C	D	E	F
X	X	X	X	?	?

Table 7: variable state

1	2	...	10	11	12
1	?	...	1		

Table 8: node state



Example - Step 4: Construction

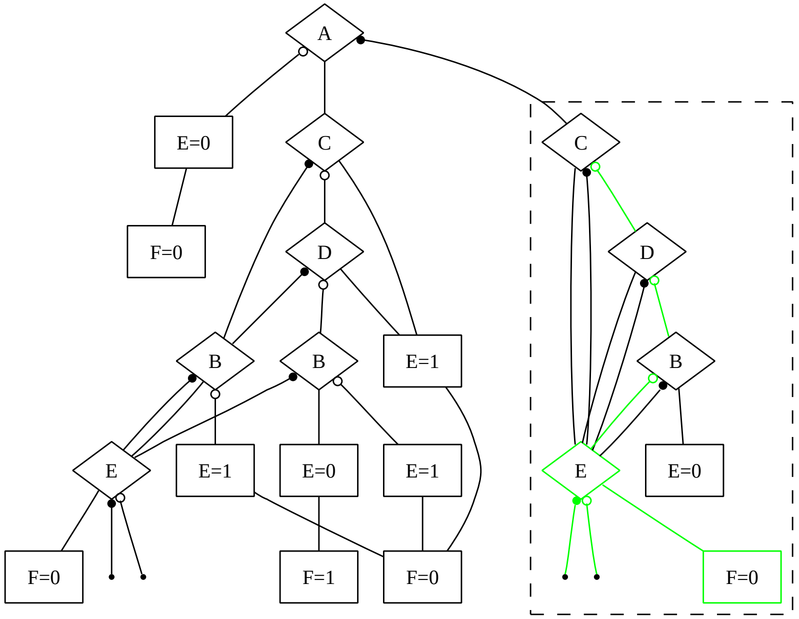
A = ?, B = C = D = 0, Node 10:

A	B	C	D	E	F
X	X	X	X	?	?

Table 9: variable state

1	2	...	10	11	12
1	?	...	1		

Table 10: node state



Example: Propagate Different Value

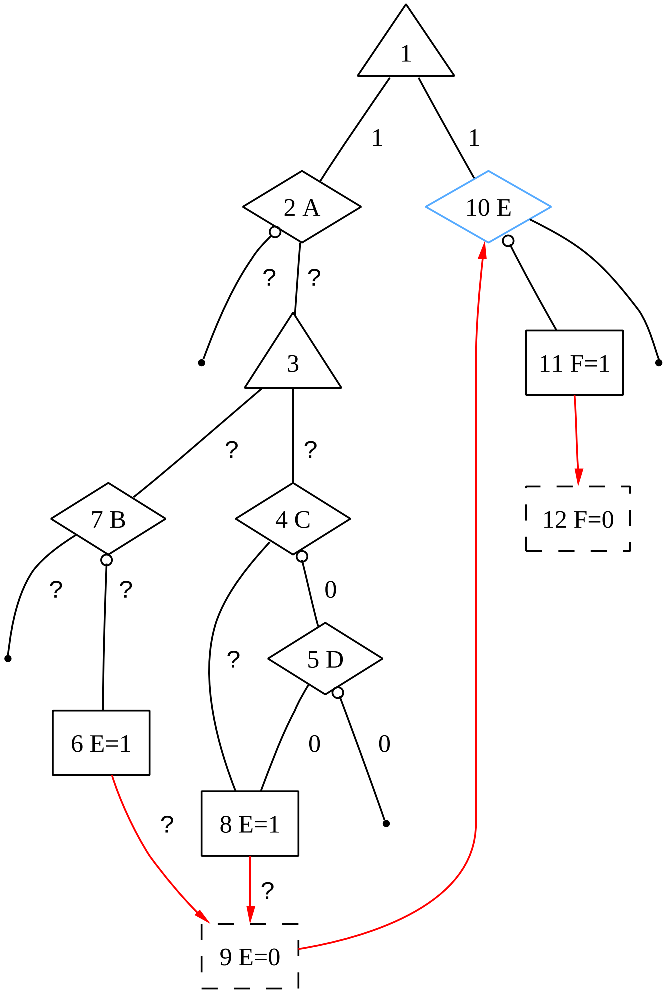
A = ?, B = D = ?, C = 1, Node 10:

A	B	C	D	E	F
X	X	X	X	?	?

Table 11: variable state

1	2	...	10	11	12
1	?	...	1		

Table 12: node state



Example: Use Same Subgraph

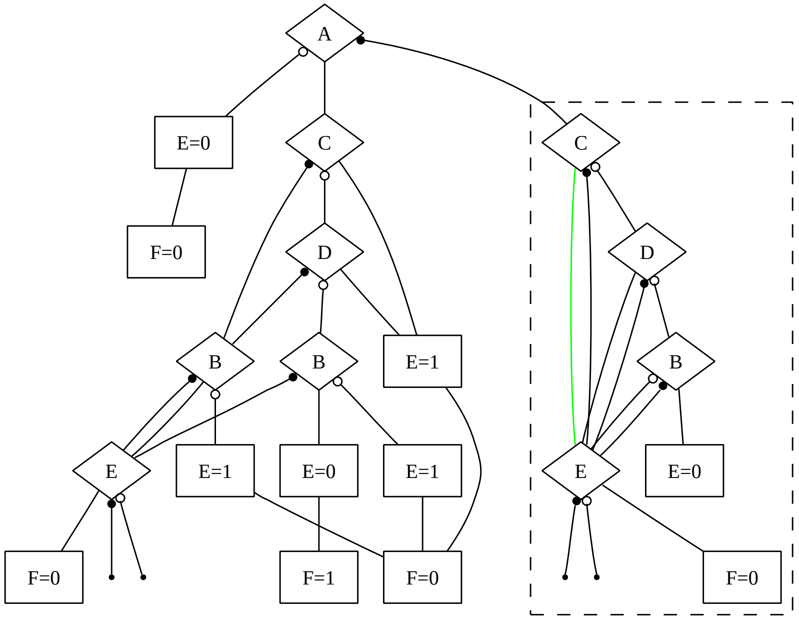
A = ?, B = ?, C = 1, D = ?

A	B	C	D	E	F
X	X	X	X	?	?

Table 13: variable state

1	2	...	10	11	12
1	?	...	1		

Table 14: node state



Example: Propagate Different Value

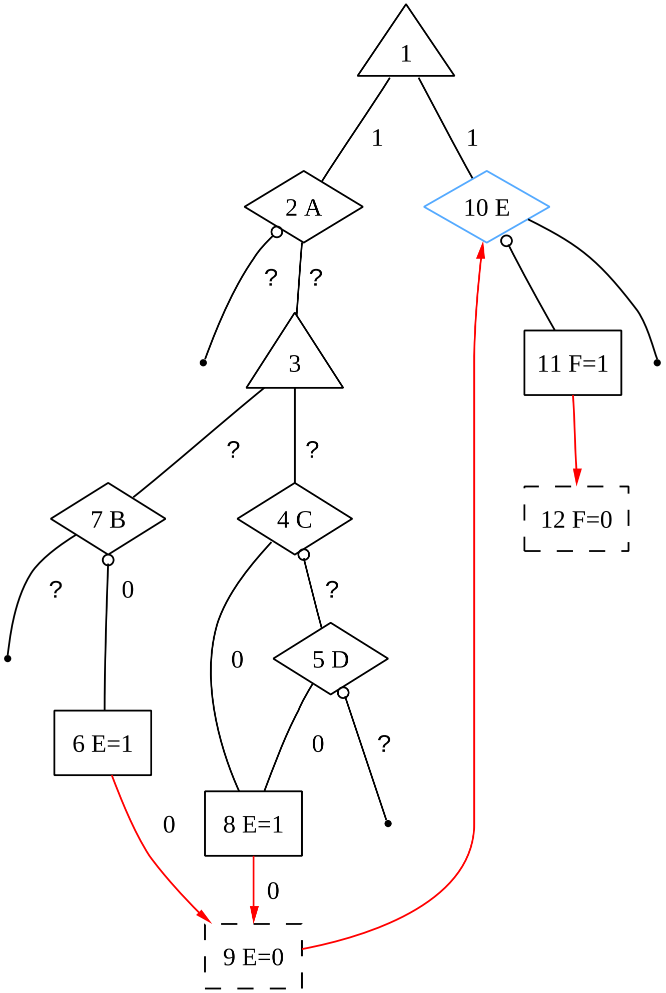
A = ?, B = 1, C = 0, D = 0

A	B	C	D	E	F
X	X	X	X	0	?

Table 15: variable state

1	2	...	10	11	12
1	?	...	1		

Table 16: node state



Example: Different Subgraph

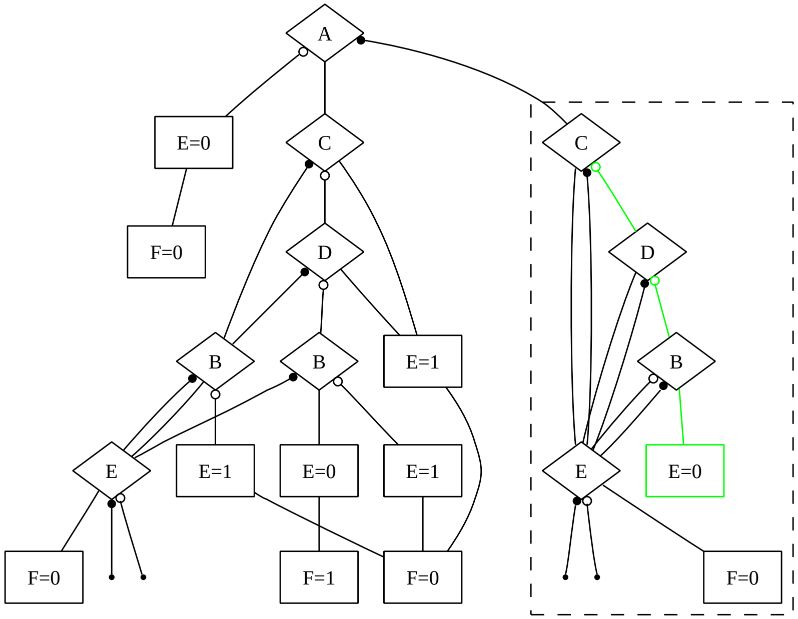
A = ?, B = 1, C = 0, D = 0

A	B	C	D	E	F
X	X	X	X	0	?

Table 17: variable state

1	2	...	10	11	12
1	?	...	1		

Table 18: node state



Experimental Result

Example	Lines	Average cycle times		
		Esterel V5	SCFG	3-Valued
comexp	88	1.67s	0.61s	0.80s
iwls3	70	1.04s	0.35s	0.26s
3vsim2	48	0.68s	0.32s	0.46s
multi3	120	1.39s	0.45s	0.47s

Conclusion

- Collect partial information;
- Build constructive graph;
- Useful for separate compilation/simulation;
- Implement on Esterel GRC, acceptable speed penalty.