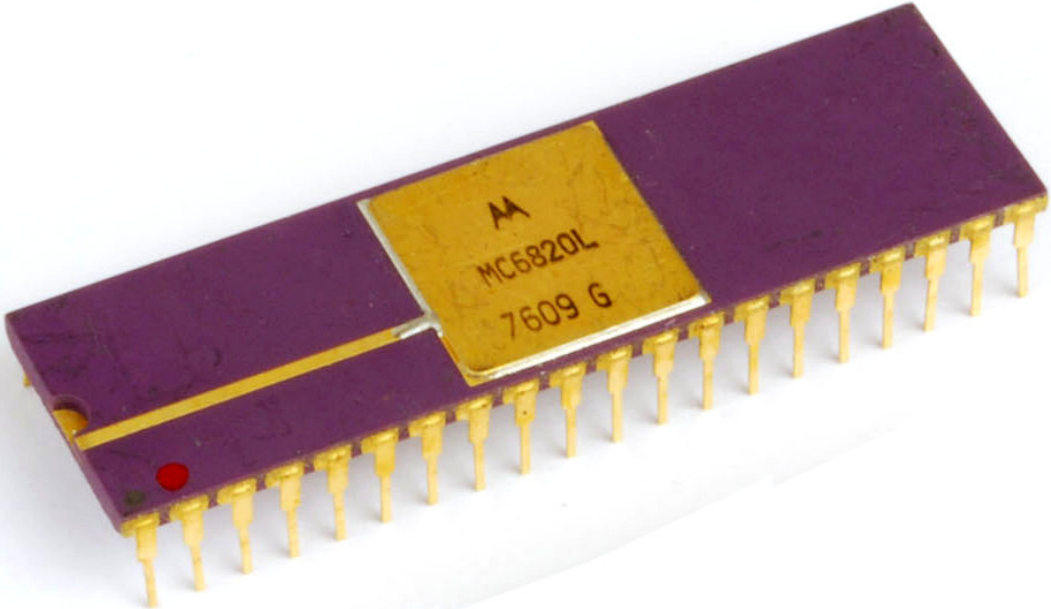

1973


AA
MC6820L
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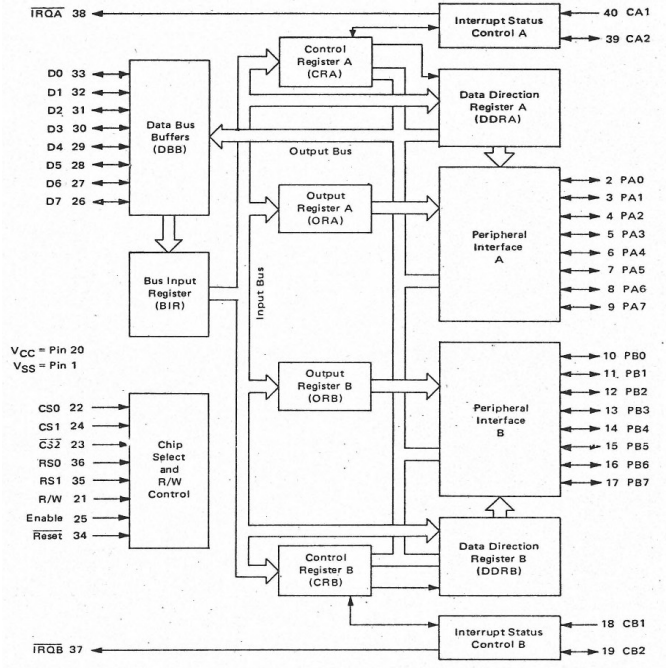
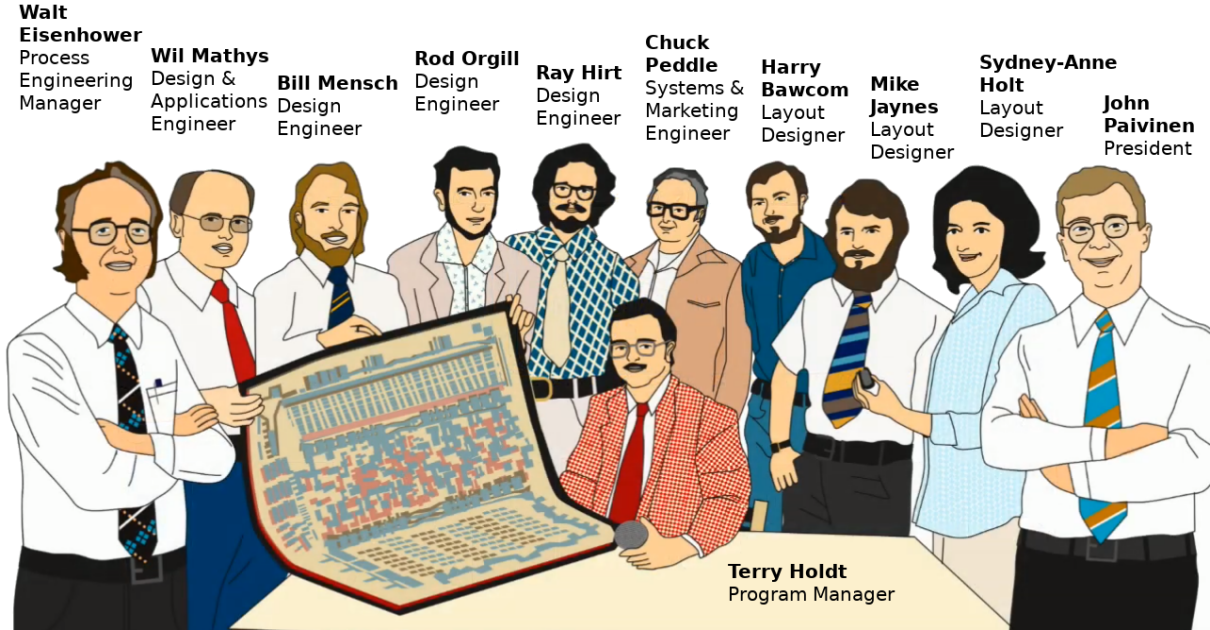

IRQA 38
Interrupt Status Control A
40 CA1
39 CA2
Control Register A (CRA)
D0 33
D1 32
D2 31
D3 30
D4 29
D5 28
D6 27
D7 26
Data Bus Buffers (DBB)
Data Direction Register A (DDRA)
Output Bus
Output Register A (ORA)
Peripheral Interface A
2 PA0
3 PA1
4 PA2
5 PA3
6 PA4
7 PA5
8 PA6
9 PA7
Bus Input Register (BIR)
Input Bus
VCC = Pin 20
VSS = Pin 1
Output Register B (ORB)
Peripheral Interface B
10 PB0
11 PB1
12 PB2
13 PB3
14 PB4
15 PB5
16 PB6
17 PB7
CS0 22
CS1 24
CS2 23
RS0 36
RS1 35
R/W 21
Enable 25
Reset 34
Chip Select and R/W Control
Data Direction Register B (DDRB)
Control Register B (CRB)
Interrupt Status Control B
18 CB1
19 CB2
IRQB 37


MC6800L
SC7711I


1974


MOS TECHNOLOGY INC


Walt Eisenhower
Process Engineering Manager
Wil Mathys
Design & Applications Engineer
Bill Mensch
Design Engineer
Rod Orgill
Design Engineer
Ray Hirt
Design Engineer
Chuck Peddle
Systems & Marketing Engineer
Harry Bawcom
Layout Designer
Mike Jaynes
Layout Designer
Sydney-Anne Holt
Layout Designer
John Paivinen
President
Terry Holdt
Program Manager

Management Team

Experienced MOS Management has been assembled to plan and execute MOS TECHNOLOGY INC. operations. A balance of business, technical and marketing skills is available within this management. They have operated successfully in the MOS field for more than two years.

PRESIDENT, JOHN PAIVINEN was most recently Vice President and General Manager of the microelectronics division of a major electronics company. Mr. Paivinen also brings experience of 16 years in the computer industry and 6 years of general management.

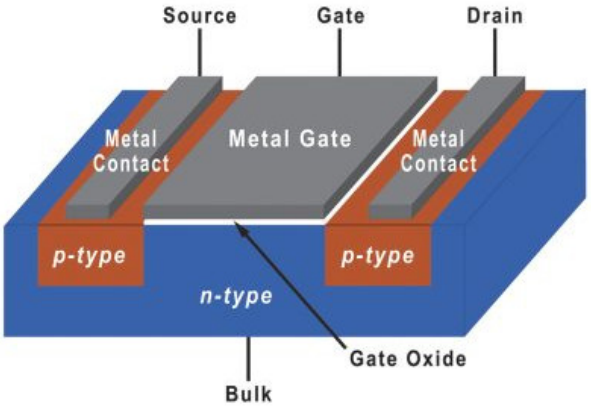
VICE PRESIDENT AND DIRECTOR OF ENGINEERING AND MANUFACTURING, DONALD McLAUGHLIN was most recently director of engineering reporting to Mr. Paivinen. He was responsible for all engineering tasks including array design, prototype production, process development, photomask production, and implementation of techniques for automatic design and array testing. Mr. McLaughlin's experience includes 12 years in data processing systems and 7 years in management.

VICE PRESIDENT AND DIRECTOR OF MARKETING, LEONARD SMITH was personally responsible for all phases of MOS marketing for a major supplier over the past 4 years. His experience in component sales, electronic systems sales and quality assurance provide a systems and quality orientation of special interest to customers. Mr. Smith has been in supervision and management positions for the past 14 years.

MANAGER OF PROCESS ENGINEERING AND TECHNOLOGY, MR. WALTER EISENHOWER brings over 14 years of pertinent experience in the fields of hybrid and monolithic integrated circuits design and fabrication. In his most recent position he was responsible for advanced process development for MOS arrays. He is experienced in all phases of planar processing, assembly techniques, passivation methods, device design, and reliability evaluation. His prior experience includes semiconductor process development at ITT, Burroughs, and Western Electric.

VICE PRESIDENT AND DIRECTOR OF OPERATIONS ADMINISTRATION, MORTON JAFFE brings management experience through the general manager level to the support functions of the company. His experience covers project management and contract negotiations on programs up to $200,000,000 in value, with overseas management experience in his last two positions.

MANAGER OF PHOTOMASK DEPARTMENT, MR. DONALD PAYNE brings to MOS TECHNOLOGY INC. 20 years of experience in the field. Eleven years as a project engineer in the advanced development department of Philco, 5 years as General Manager of Phototronics Division of Biskay, Photomask Manufacturers, and 2 years as Manager of the Photomask Department of General Instrument Microelectronics Division.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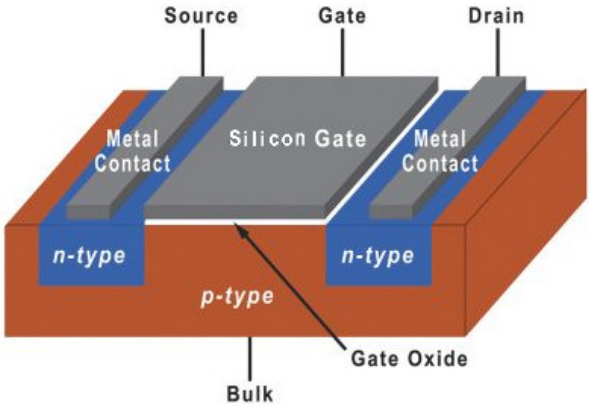
Gate
Drain
Metal Contact
Metal Gate
Metal Contact
p-type
p-type
n-type
Gate Oxide
Bulk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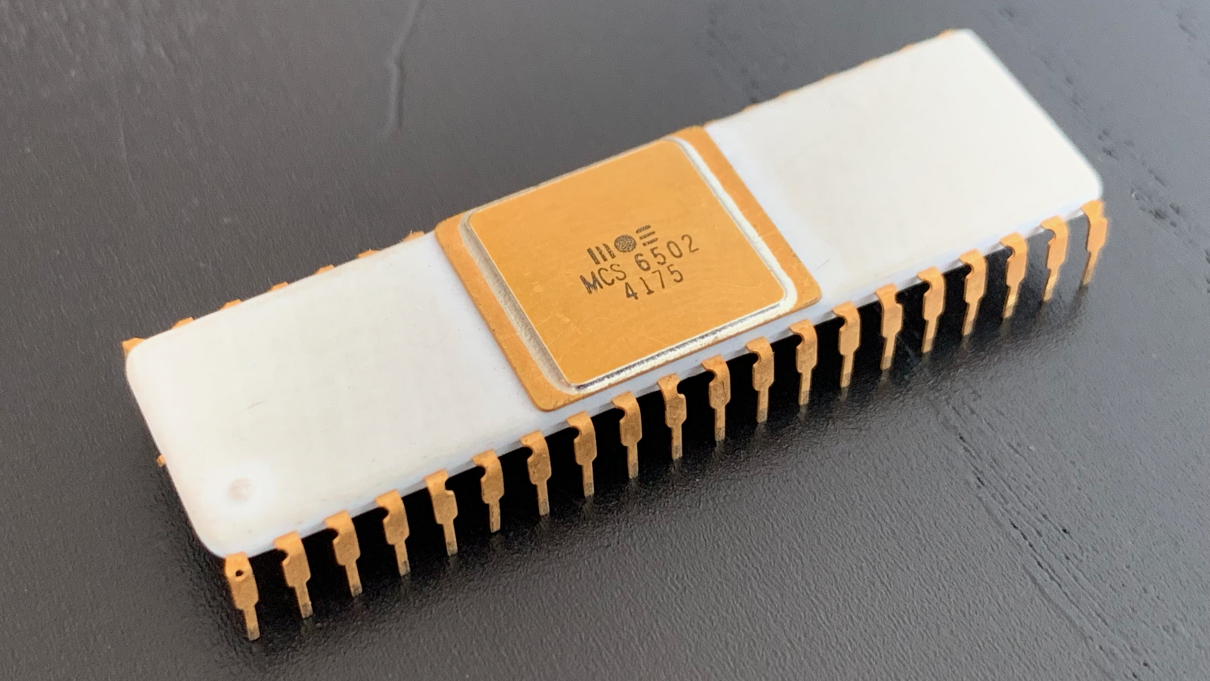
Metal Contact
n-type
n-type
p-type
Gate Oxide
Bulk


1975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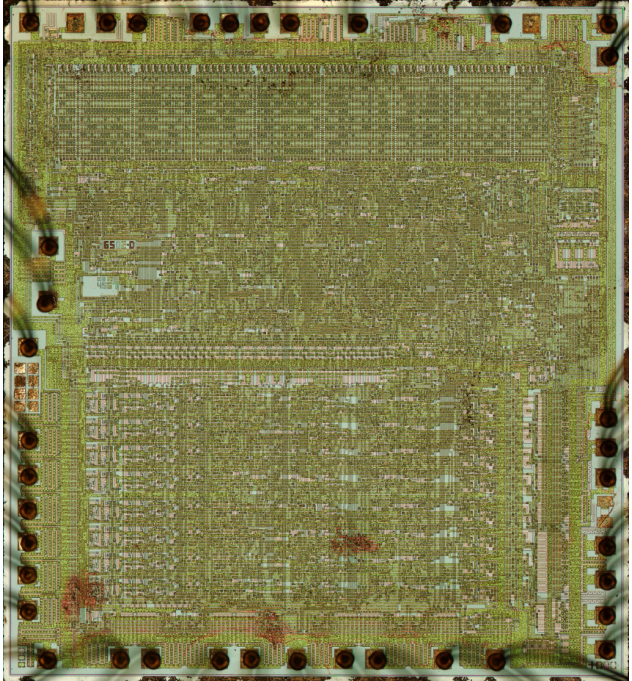
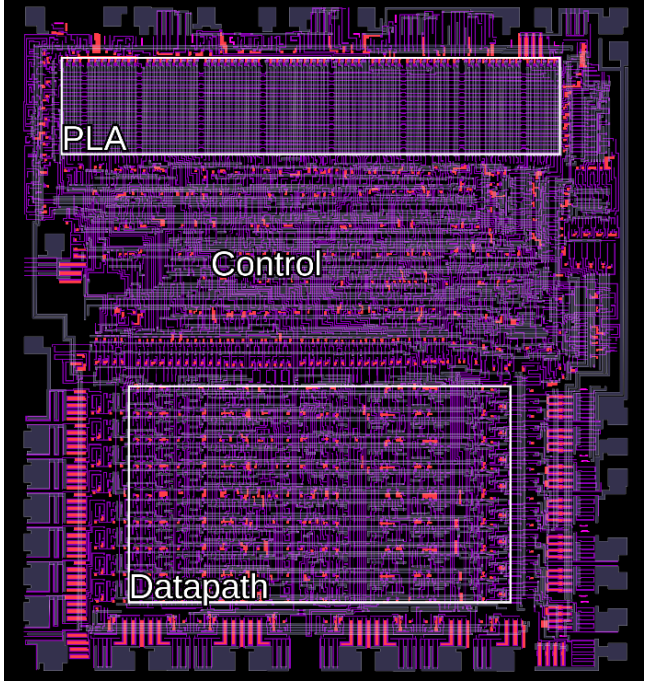
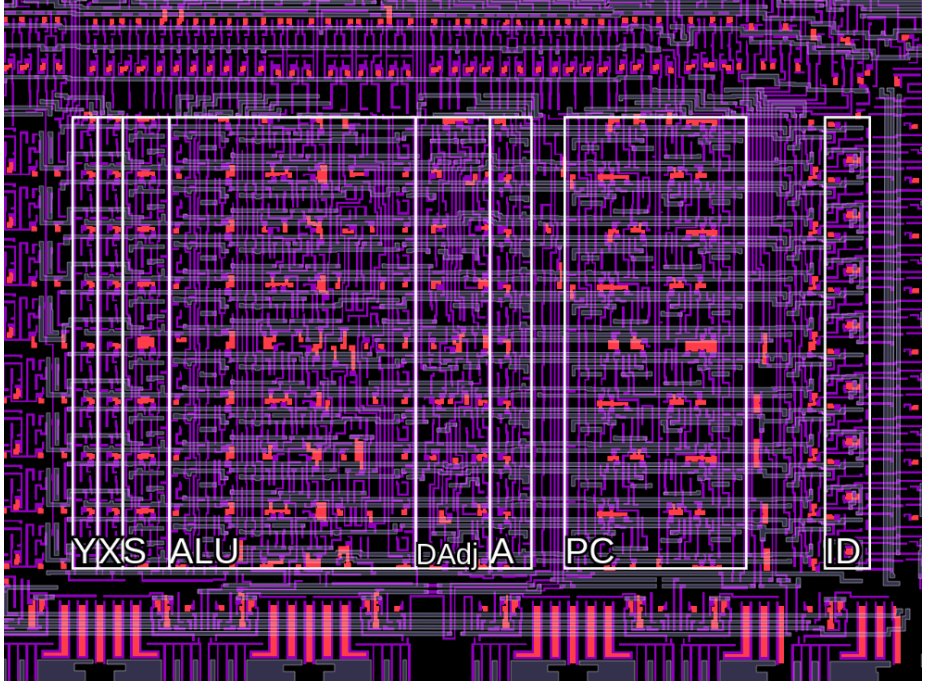



PLA
Control
Datapath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THE
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OLIVIA NEWTO
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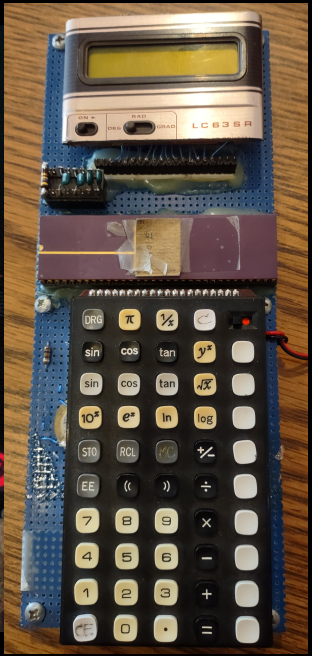
CARTOONIST, AND THIS
IS MY CAT,
GARFIELD.
1978


DUNES
DREAM STREET
CASINO
Dunes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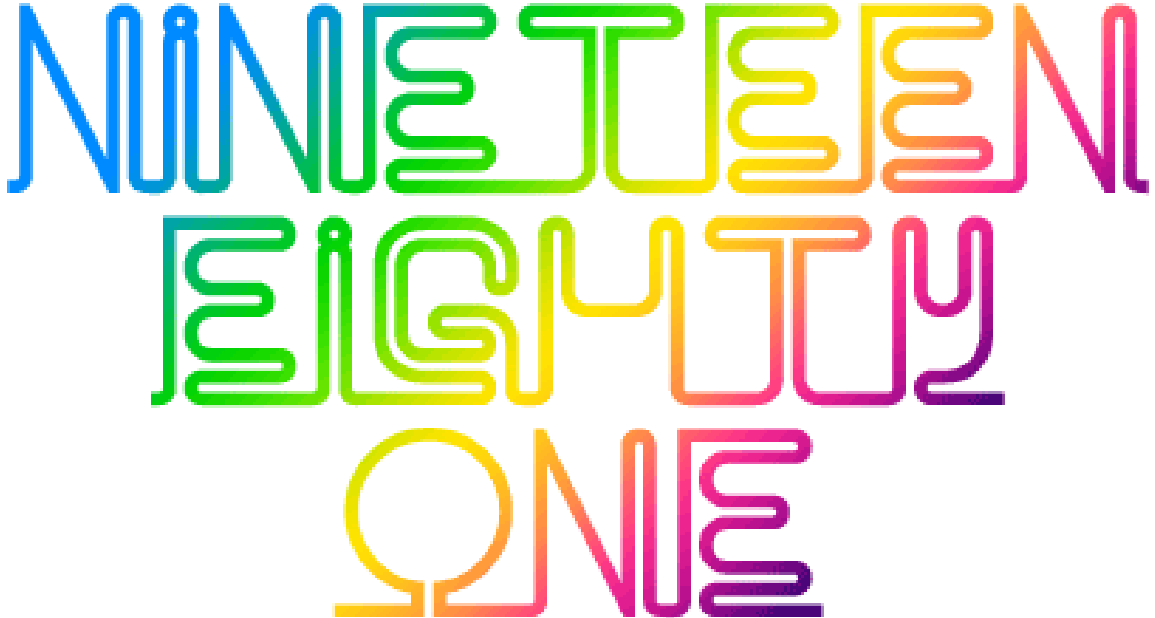
NINETEEN
EIGHTY
ONE


INTER-TEL
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SYS HOLD
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6
ABC 2
DEF 3
GHI 4
JKL 5
MNO 6
PRS 7
TUV 8
WXY 9
OPER 0
CNF
SPDL
PAGE
E-PAGE
INTER-TEL/GLX


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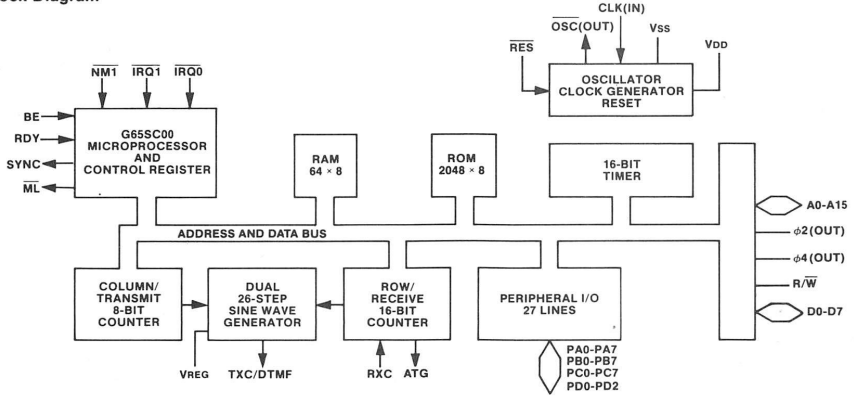
GTE μ
P3300 14PE
G65SC150PE-2
8722
UC2
65SC151
J10

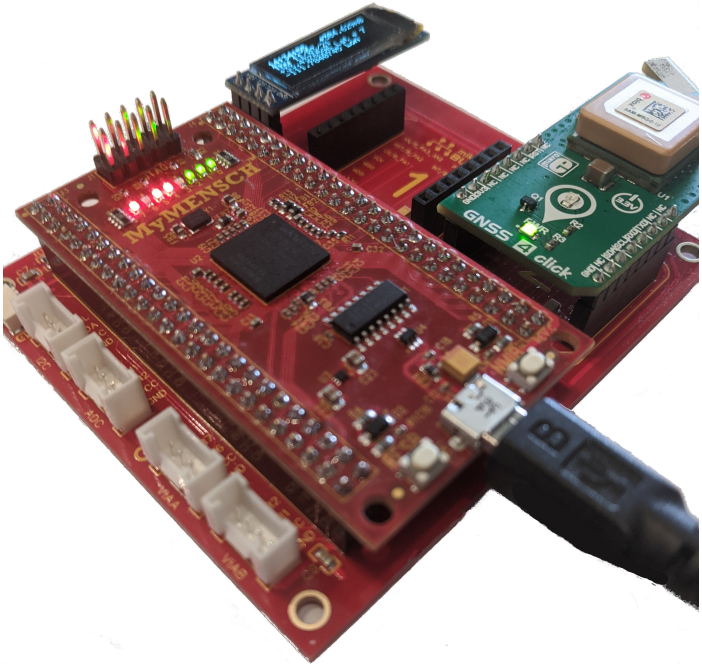
G65SC150

Microcircuits

CMOS Communications Terminal Unit (Telecommunication Microcomputer)

Block Diagram

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