

NAME

`cec` – The Columbia Esterel Compiler

SYNOPSIS

`cec [--blif | --verilog | --sm] [options...] file.strl`

`cec [--blif | --verilog] [options...] file.sm`

DESCRIPTION

The `cec` command invokes the compiler, translating Esterel source code (suffix `.strl`) into a circuit representation, in either the BLIF format accepted by the `sis(1)` logic optimizer from Berkeley, or the Verilog language. In the most basic form,

`cec myfile.strl`

compiles the Esterel source file `myfile.strl` into the BLIF file `myfile.blif`. Verilog, in a file called `myfile.v` may be generated by providing an option:

`cec --verilog myfile.strl`

All local state machines are given a default encoding that can be manually overridden by supplying a `.sm` file. This is done by asking `cec` to generate an `.sm` file, editing it, then asking `cec` to finish its job, e.g.,

`cec --sm myfile.strl`

Edit the file myfile.sm

`cec myfile.sm`

By default, this generates a `.blif` file. Verilog may also be generated by providing an option:

`cec --verilog myfile.sm`

OPTIONS

Output language options

--blif Generate a `.blif` file as output. This is the default.

--verilog

Generate a `.v` (Verilog) file as output.

--sm Generate a `.sm` (state machine) file as output. This file may be edited and later resupplied to `cec` to complete the compilation process and produce either Verilog or BLIF.

Optimization options

--sis Invoke the `sis(1)` logic synthesis system as part of the compilation process. By default, this runs the standard `script.rugged` optimization script, but this may be changed using the following option.

--sis-script *script*

Specify the script invoked by `sis(1)` during optimization. This implies **--sis**

Output control options

-B *basename*

Specify the basename of generated files. This normally defaults to the basename of the given `.strl` file, but may be specified explicitly using this option.

-D *directory*

Specify the destination directory for generated files. This defaults to the current working directory.

-K

Keep all intermediate files; by default all are deleted after compilation is complete. Most are in XML format. This is useful mostly to developers.

—keep *extension*

Keep the intermediate file with the given extension. Invoking **cec** **—keep** alone lists the possible extensions. Multiple **—keep** directives may be issued.

Miscellaneous options

—h

—help Print a usage summary.

—version

Print the version of the compiler.

—v

—verbose

Enable verbose mode. Report each internal command as it is executed.

—logfile *file*

Generate a log file with the given name. This contains version information, the command line that invoked the compiler, and the list of commands invoked during the compilation process.

—eachcmd *cmd*

Specify a command to precede each command invoked by the compiler. For example, **—eachcmd time** times each internally-executed command. Useful mostly to developers.

—pdgblifargs *args*

Specify additional arguments to be passed directly to the **pdgblif** pass. Useful mostly to developers.

BUGS

Cec does not support many parts of the Esterel V5 language, including the *pre* operator, variables, external types, functions, procedures, and tasks.

The generated circuit can always be improved.

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SEE ALSO

<<http://www.cs.columbia.edu/~sedwards/>>

The CMA/INRIA Esterel V5 compiler, available from <<http://www.esterel-technologies.com/>>

The Esterel V5 Language Primer

Gerard Berry, *The Constructive Semantics of Esterel*

The Icarus Verilog simulator/synthesizer <<http://www.icarus.com/eda/verilog/>>

The **sis**(1) logic synthesis system.