Mescal Architecture Model

Scott J Weber
Kurt Keutzer

Mescal Views

![Diagram of Mescal Views]

Resource | 0 | 1 | 2 | 3
---|---|---|---|---
RegFile | X | X | X |
ALU | X | X |

ADD:

- Instruction semantics
- Code generator
- Resource usage
- Register classes
- Compiler View
Architecture View

- PtolemyII and Vergil as the base
- Expandable library of common micro-architecture components
- Strongly-typed visual language with type and domain polymorphic actors
- Exploits bit-level and instruction-level concurrency
- Actors have cycle delays
- Conductor handles control
  - Output controls dataflow actors
  - Control implicitly synchronized

ISA View

- User defines an instruction by giving it a name and specifying the resources it uses
- Static timing analysis determines the timing
  - Instructions are synchronized from the Conductor
- Simplifies ISA development
- Correct by construction
- Information is used to create the simulator and can be used by the compiler for scheduling
Simulator View

- Generate an AST of the model
- Knowledge of the MOC and semantics of PtolemyII allows code generation from the AST
- Code generated is a compiled simulator of the model

while (iterations) {
    decode instruction and send tokens
    if (a enabled)
        execute a
    if (b enabled)
        execute b
    if (c enabled)
        execute c
    // move data through the pipeline
    move present state to next state
}

24 September 99

Memory View

- For memory architecture exploration
- Views memory as a table and accessing ports

- Port and read/write prioritization determine access order
- Variable delays in cycles

24 September 99
Compiler View

- Size and features of the register files
- Expose intrinsics and memory features
- Behavioral description of the instruction (like ISDL/nML)

Model of Computation

- Implicit actors added with knowledge of the MOC
- As a dataflow model, there is one token per edge
  - Static schedule except for a conditional enable
  - Centralized control through the Conductor produces the tokens including enables at the correct time
  - Token, enable, and stall set generated on each cycle by identifying the issued instruction

* Stall signals not shown but would come from the Conductor too
Mapping to the Middle

Architectural Exploration